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# AO4286

## 100V N-Channel MOSFET

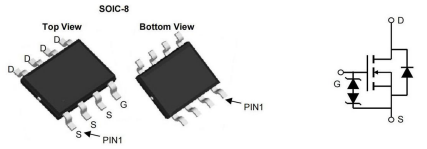
### General Description

The AO4286 uses trench MOSFET technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$, Ciss and Coss. This device is ideal for boost converters and synchronous rectifiers for consumer, telecom, industrial power supplies and LED backlighting.

### Product Summary

| | |
|---|---|
| $V_{DS}$ | 100V |
| $I_D$ (at $V_{GS}$=10V) | 4A |
| $R_{DS(ON)}$ (at $V_{GS}$=10V) | < 68mΩ |
| $R_{DS(ON)}$ (at $V_{GS}$=4.5V) | < 92mΩ |

100% UIS Tested




| Orderable Part Number | Package Type | Form | Minimum Order Quantity |
|---|---|---|---|
| | SO-8 | Tape & Reel | 3000 |

**Absolute Maximum Ratings $T_A$=25℃ unless otherwise noted**

| Parameter | | Symbol | Maximum | Units |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 100 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current | $T_C$=25℃ | $I_D$ | 4 | A |
| | $T_C$=70℃ | | 3 | |
| Pulsed Drain Current [C] | | $I_{DM}$ | 25 | |
| Avalanche Current [C] | | $I_{AS}$ | 4 | A |
| Avalanche energy L=0.1mH [C] | | $E_{AS}$ | 0.8 | mJ |
| Power Dissipation [B] | $T_A$=25℃ | $P_D$ | 2.5 | W |
| | $T_A$=70℃ | | 1.6 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 150 | ℃ |

**Thermal Characteristics**

| Parameter | | Symbol | Typ | Max | Units |
|---|---|---|---|---|---|
| Maximum Junction-to-Ambient [A] | t ≤ 10s | $R_{\theta JA}$ | 42 | 50 | ℃/W |
| Maximum Junction-to-Ambient [A D] | Steady-State | | 70 | 85 | ℃/W |
| Maximum Junction-to-Lead | Steady-State | $R_{\theta JL}$ | 20 | 30 | ℃/W |

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**Electrical Characteristics ($T_J$=25℃ unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=250μA, $V_{GS}$=0V | 100 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=100V, $V_{GS}$=0V | | | 1 | μA |
| | | $T_J$=55℃ | | | 5 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$=±20V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_D$=250μA | 1.7 | 2.25 | 2.9 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}$=10V, $V_{DS}$=5V | 25 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=10V, $I_D$=4A | | 55.5 | 68 | mΩ |
| | | $T_J$=125℃ | | 104 | 127 | |
| | | $V_{GS}$=4.5V, $I_D$=3A | | 72.5 | 92 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=5V, $I_D$=4A | | 13 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=1A,$V_{GS}$=0V | | 0.76 | 1 | V |
| $I_S$ | Maximum Body-Diode Continuous Current | | | | 3 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=50V, f=1MHz | | 390 | | pF |
| $C_{oss}$ | Output Capacitance | | | 30 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 3 | | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | | 7 | | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$(10V) | Total Gate Charge | $V_{GS}$=10V, $V_{DS}$=50V, $I_D$=4A | | 5.8 | 10 | nC |
| $Q_g$(4.5V) | Total Gate Charge | | | 2.8 | 5 | nC |
| $Q_{gs}$ | Gate Source Charge | | | 1.1 | | nC |
| $Q_{gd}$ | Gate Drain Charge | | | 1.2 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=10V, $V_{DS}$=50V, $R_L$=12.5Ω, $R_{GEN}$=3Ω | | 6 | | ns |
| $t_r$ | Turn-On Rise Time | | | 2.5 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 18 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 2.5 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=4A, dI/dt=500A/μs | | 15 | | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=4A, dI/dt=500A/μs | | 53 | | nC |

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initial$T_J$=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

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## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

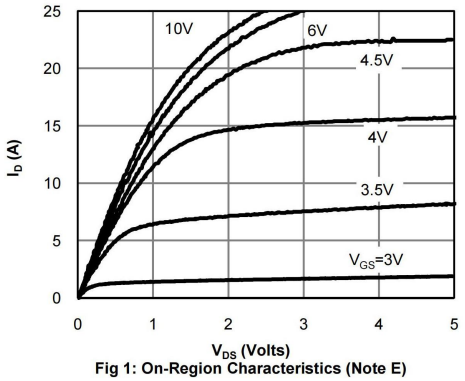



Fig 1: On-Region Characteristics (Note E)

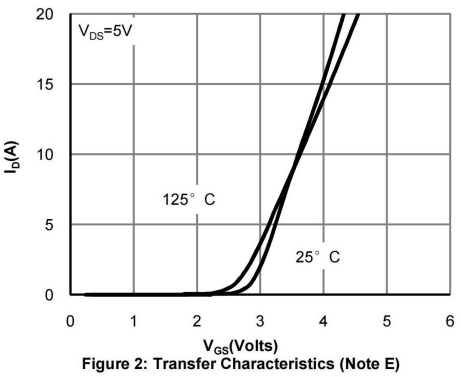



Figure 2: Transfer Characteristics (Note E)

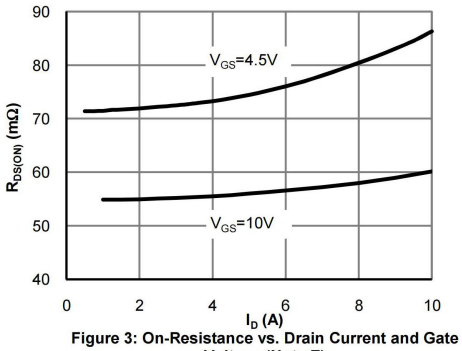



Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

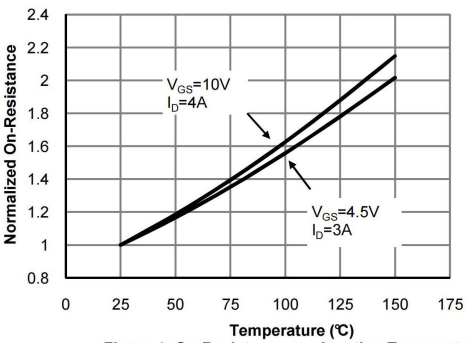



Figure 4: On-Resistance vs. Junction Temperature (Note E)

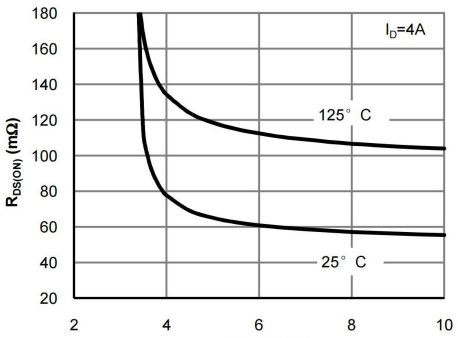



Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

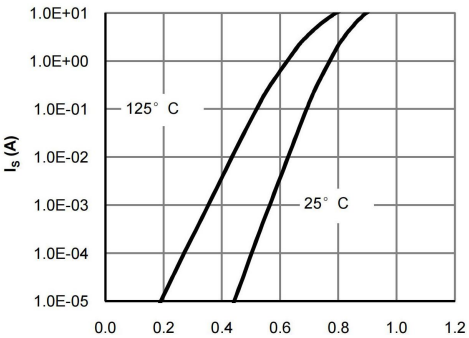



Figure 6: Body-Diode Characteristics (Note E)

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## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

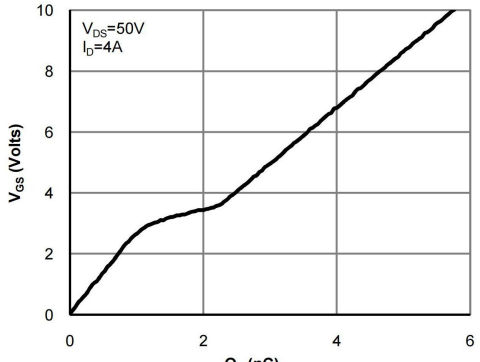



Figure 7: Gate-Charge Characteristics

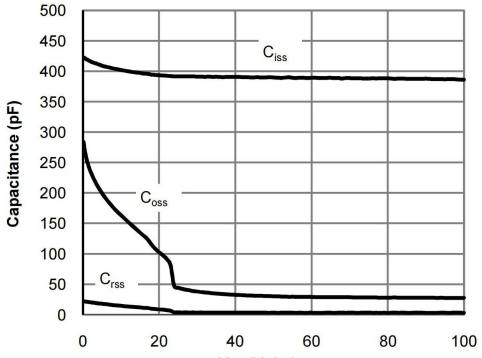



Figure 8: Capacitance Characteristics

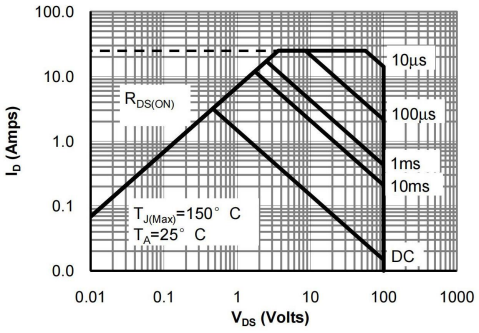



Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

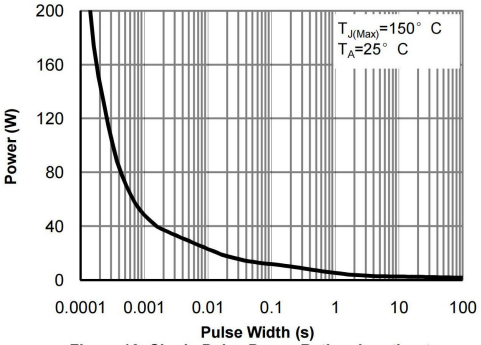



Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

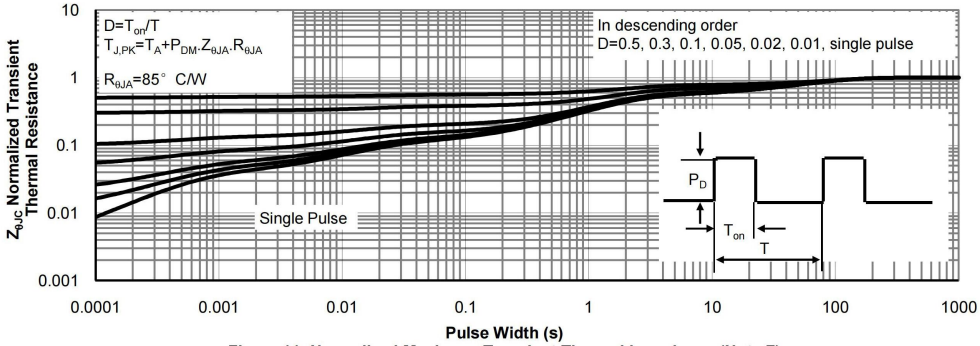
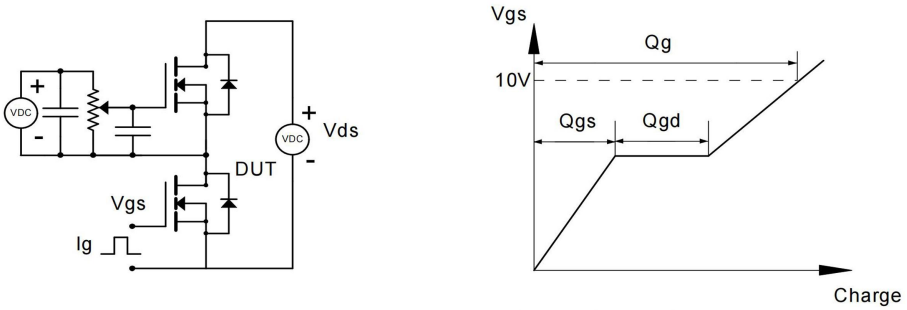


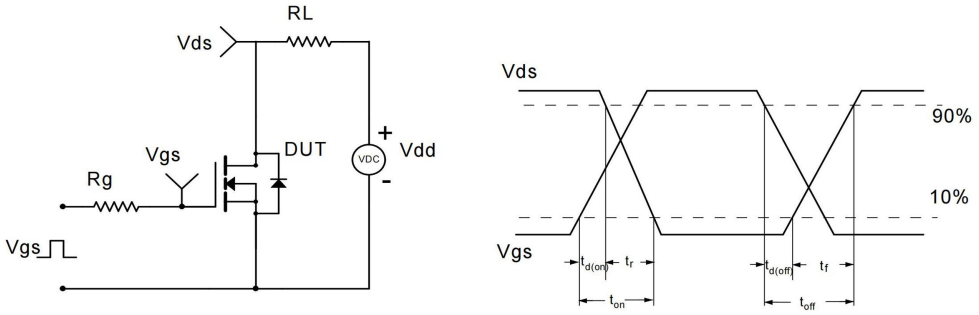

Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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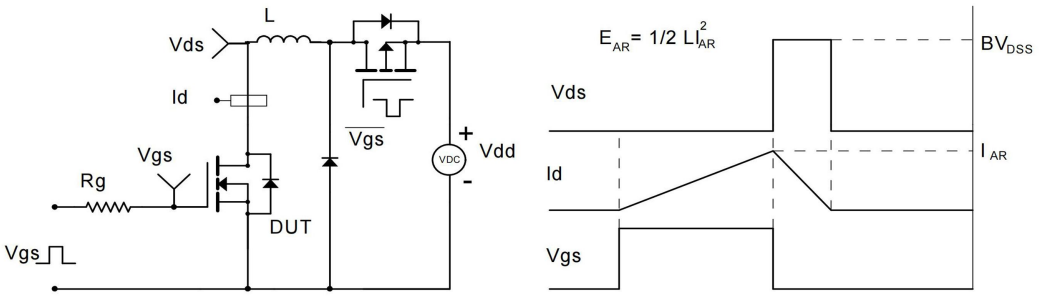
Gate Charge Test Circuit & Waveform




Resistive Switching Test Circuit & Waveforms




Unclamped Inductive Switching (UIS) Test Circuit & Waveforms




Diode Recovery Test Circuit & Waveforms

