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AO4421

60V P-Channel MOSFET

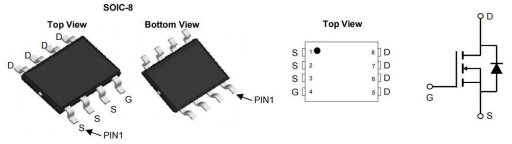
General Description

The AO4421 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

Product Summary

V_{DS}	-60V
I_D (at V_{GS}=-10V)	-6.2A
$R_{DS(ON)}$ (at V_{GS}=-10V)	< 40mΩ
$R_{DS(ON)}$ (at V_{GS} = -4.5V)	< 50mΩ

100% UIS Tested
100% R_g Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
	SO-8	Tape & Reel	3000

Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [A]	T_A=25℃	I_D	-6.2	A
	T_A=70℃		-5	
Pulsed Drain Current [B]		I_{DM}	-40	
Power Dissipation [A]	T_A=25℃	P_D	3.1	W
	T_A=70℃		2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	24	40	℃/W
Maximum Junction-to-Ambient [A]	Steady-State		54	75	℃/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	21	30	℃/W

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Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250μA, V_{GS}=0V	-60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-48V, V_{GS}=0V			-1	μA
		T_J=55℃			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250μA	-1	-2	-3	V
$I_{D(ON)}$	On state drain current	V_{GS}=-10V, V_{DS}=-5V	-40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-6.2A		32	40	mΩ
		T_J=125℃		53	70	
		V_{GS}=-4.5V, I_D=-5A		40	50	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-6.2A		18		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.74	-1	V
I_S	Maximum Body-Diode Continuous Current				-4.2	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-30V, f=1MHz		2417	2900	pF
C_{oss}	Output Capacitance			179		pF
C_{rss}	Reverse Transfer Capacitance			120		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		1.9	2.3	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge (10V)	V_{GS}=-10V, V_{DS}=-30V, I_D=-6.2A		46.5	55	nC
Q_g(4.5V)	Total Gate Charge (4.5V)			22.7		nC
Q_{gs}	Gate Source Charge			9.1		nC
Q_{gd}	Gate Drain Charge			9.2		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-30V, R_L=4.7Ω, R_{GEN}=3Ω		9.8		ns
t_r	Turn-On Rise Time			6.1		ns
$t_{D(off)}$	Turn-Off DelayTime			44		ns
t_f	Turn-Off Fall Time			12.7		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-6.2A, dI/dt=100A/μs		34	42	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-6.2A, dI/dt=100A/μs		47		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25℃. The value in any a given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6,12,14 are obtained using 80 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25℃. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL

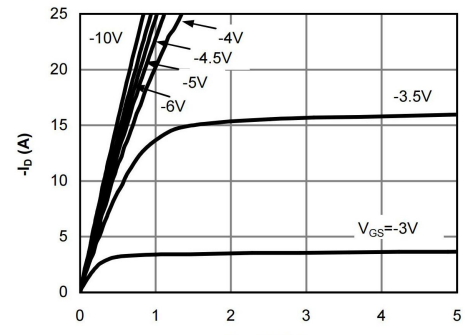


Fig 1: On-Region Characteristics

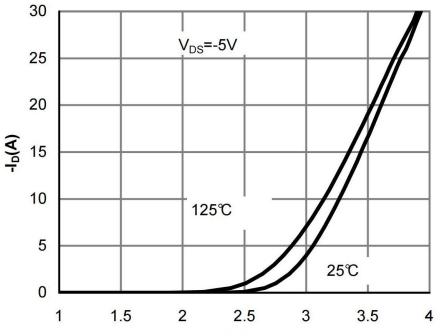


Figure 2: Transfer Characteristics

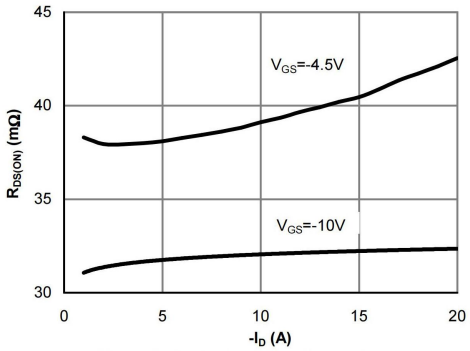


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

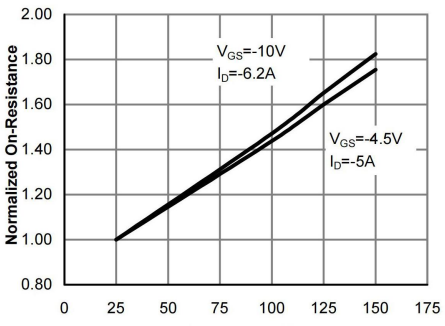


Figure 4: On-Resistance vs. Junction Temperature

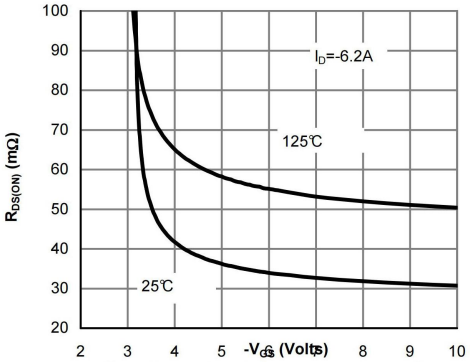


Figure 5: On-Resistance vs. Gate-Source Voltage

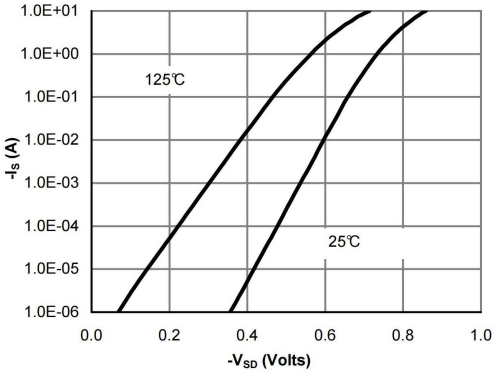


Figure 6: Body-Diode Characteristics

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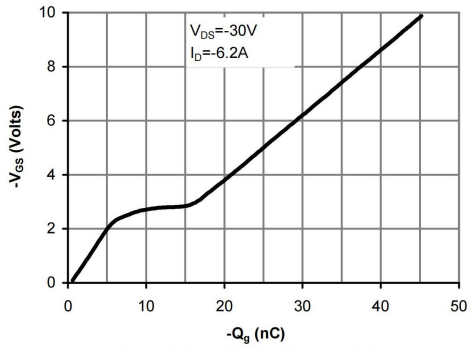


Figure 7: Gate-Charge Characteristics

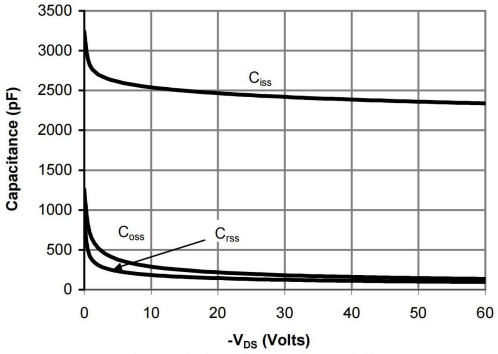


Figure 8: Capacitance Characteristics

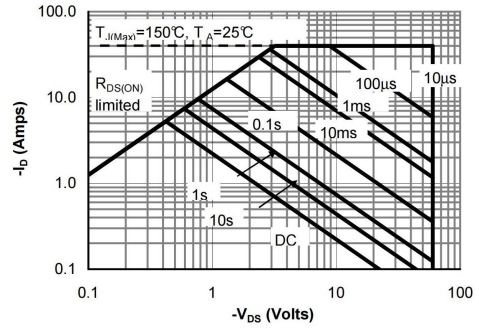


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

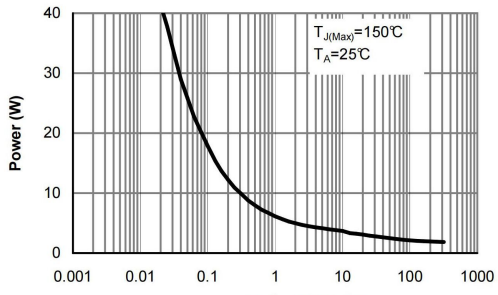


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

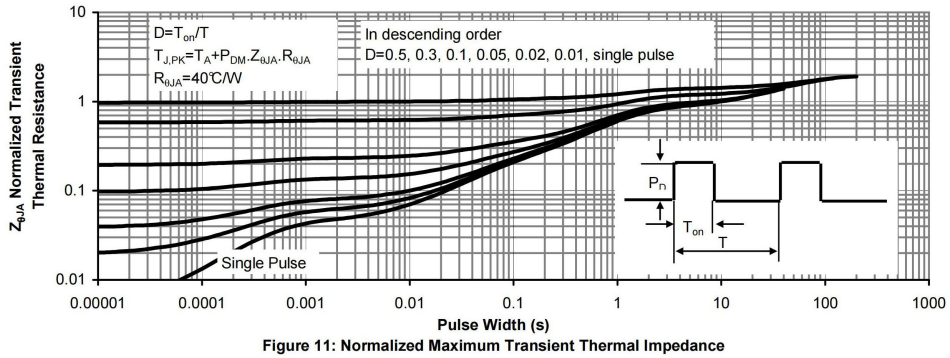
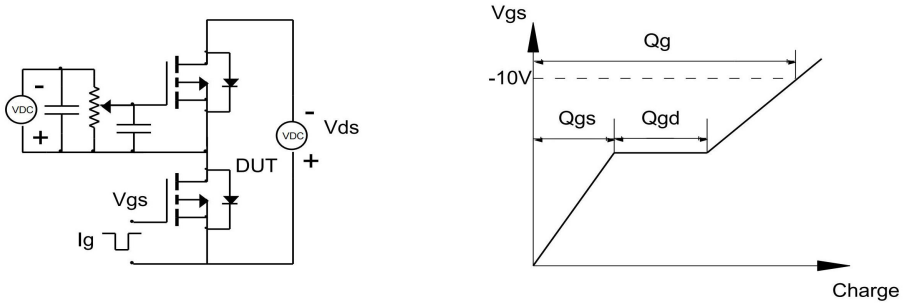


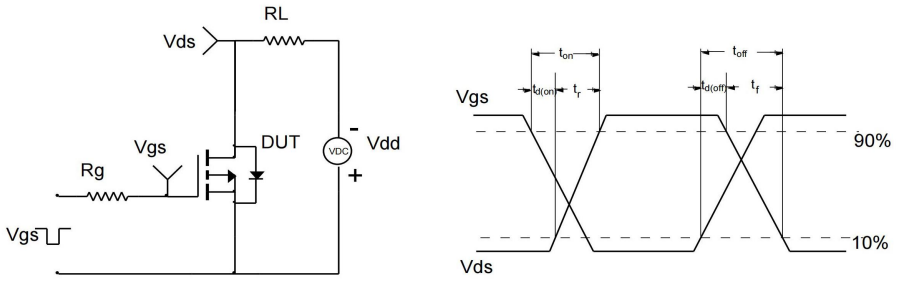
Figure 11: Normalized Maximum Transient Thermal Impedance

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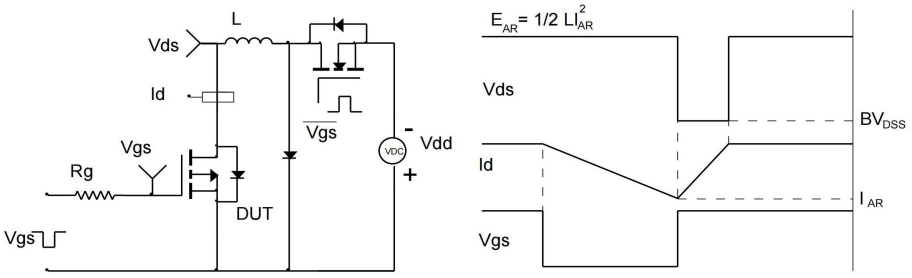
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

