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AO4496

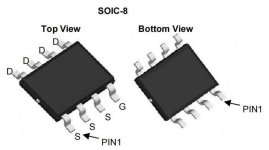
General Description

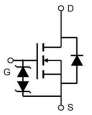
The AO4496 uses advanced trench technology to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use as a DC-DC converter application.

Product Summary

V_{DS} (V) = 30V
I_D = 10A (V_{GS} = 10V)
$R_{DS(ON)}$ < 19.5mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ < 26mΩ (V_{GS} = 4.5V)

100% UIS Tested
100% Rg Tested





Orderable Part Number	Package Type	Form	Minimum Order Quantity
	SO-8	Tape & Reel	3000

Absolute Maximum Ratings T_J=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [A]	T_A=25°C	I_D	10	A
	T_A=70°C		7.5	
Pulsed Drain Current [B]		I_{DM}	50	
Avalanche Current [G]		I_{AR}	17	
Repetitive avalanche energy L=0.1mH [G]		E_{AR}	14	mJ
Power Dissipation [A]	T_A=25°C	P_D	3.1	W
	T_A=70°C		2.0	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	31	40	°C/W
Maximum Junction-to-Ambient [A]	Steady State		59	75	°C/W
Maximum Junction-to-Lead [C]	Steady State	$R_{\theta JL}$	16	24	°C/W

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Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 30V, V_{GS} = 0V			1	μA
		T_J = 55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250μA	1.4	1.8	2.5	V
$I_{D(ON)}$	On state drain current	V_{GS} = 10V, V_{DS} = 5V	50			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10V, I_D = 10A		16	19.5	mΩ
		T_J=125°C		24	29	
		V_{GS} = 4.5V, I_D = 7.5A		21	26	
g_{FS}	Forward Transconductance	V_{DS} = 5V, I_D = 10A		30		S
V_{SD}	Diode Forward Voltage	I_S = 1A,V_{GS} = 0V		0.76	1	V
I_S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		550	715	pF
C_{oss}	Output Capacitance			110		pF
C_{rss}	Reverse Transfer Capacitance			55		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	3	4	4.9	Ω
SWITCHING PARAMETERS						
Q_g (10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=10A		9.8	13	nC
Q_g (4.5V)	Total Gate Charge			4.6	6.1	nC
Q_{gs}	Gate Source Charge			1.8		nC
Q_{gd}	Gate Drain Charge			2.2		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L= 1.5Ω, R_{GEN}=3Ω		5		ns
t_r	Turn-On Rise Time			3.2		ns
$t_{D(off)}$	Turn-Off DelayTime			24		ns
t_f	Turn-Off Fall Time			6		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=10A, dI/dt=500A/μs		22	29	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=10A, dI/dt=500A/μs		14		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A = 25° C. The value in any given application depends on the user's specific board design.
B: Repetitive rating, pulse width limited by junction temperature.
C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
D. The static characteristics in Figures 1 to 6 are obtained using t ≤ 300μs pulses, duty cycle 0.5% max.
E. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

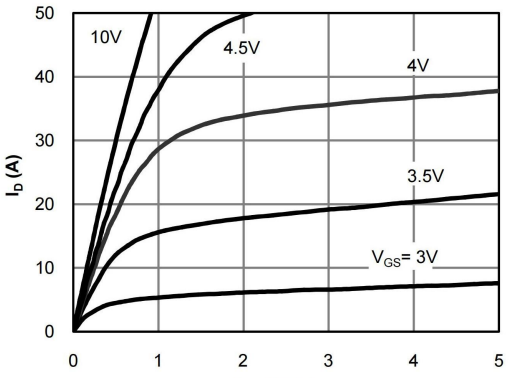


Figure 1: On-Region Characteristics

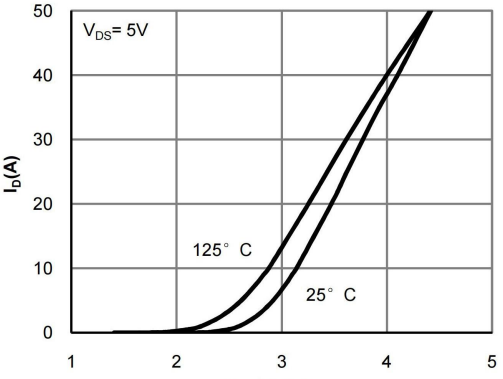
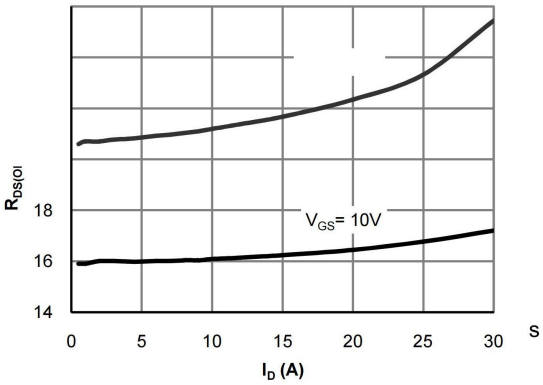


Figure 2: Transfer Characteristics



Gate Voltage

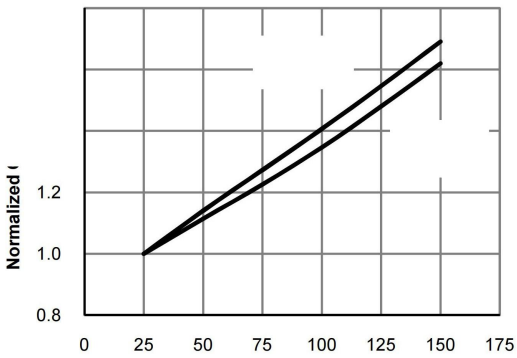


Figure 4: On-Resistance vs. Junction Temperature

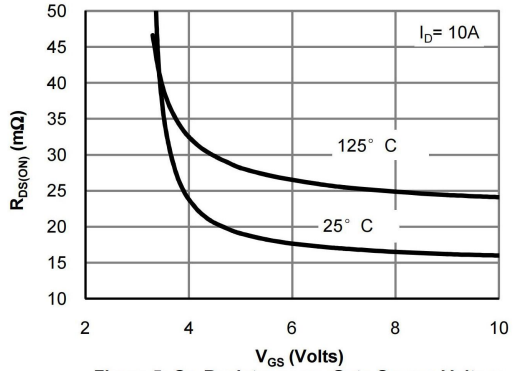


Figure 5: On-Resistance vs. Gate-Source Voltage

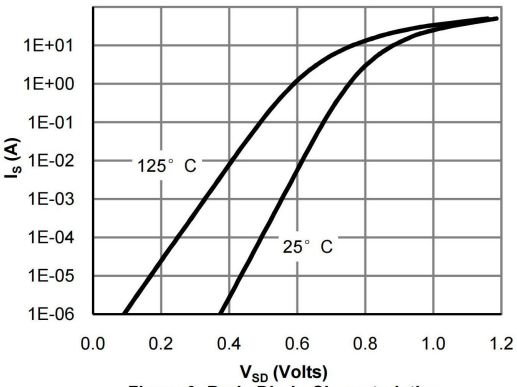


Figure 6: Body-Diode Characteristics

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

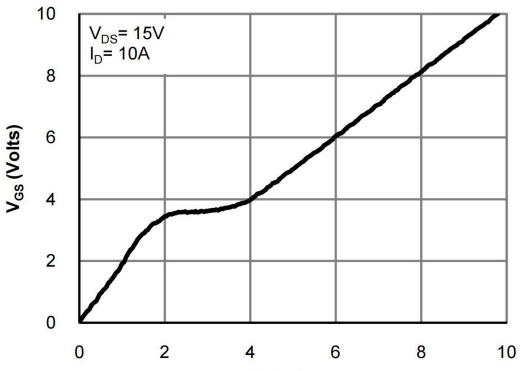


Figure 7: Gate-Charge Characteristics

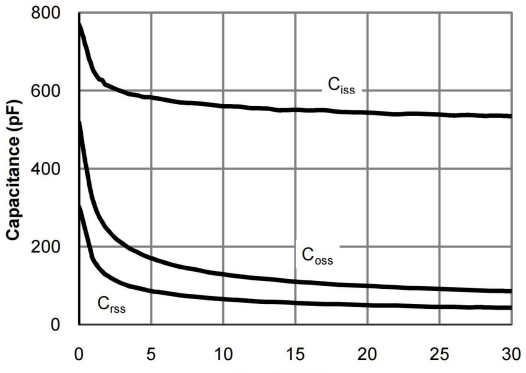


Figure 8: Capacitance Characteristics

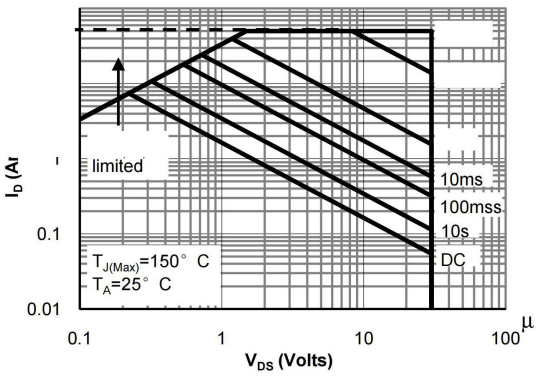


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

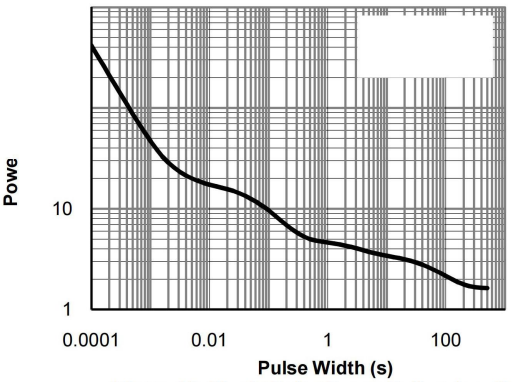


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

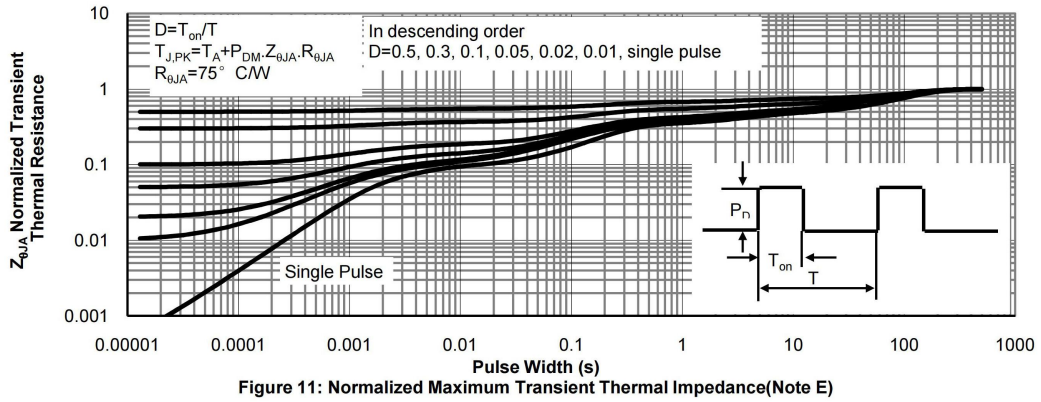
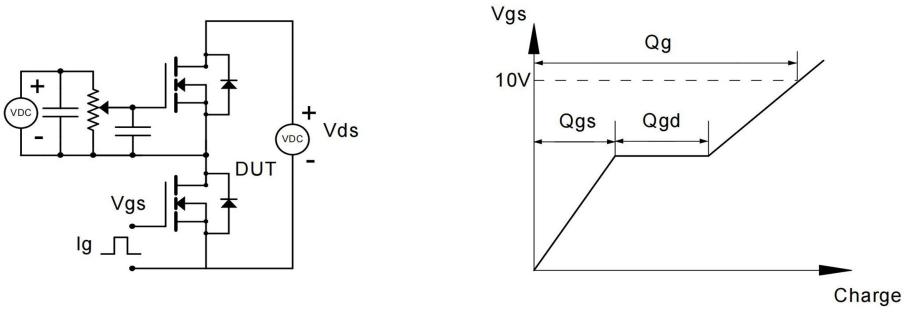


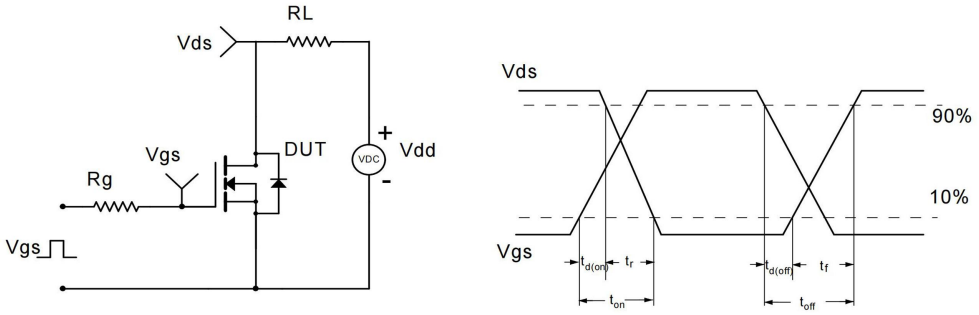
Figure 11: Normalized Maximum Transient Thermal Impedance(Note E)

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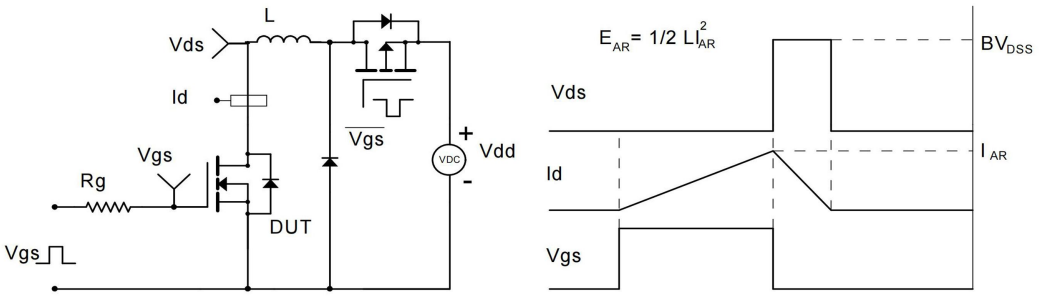
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

