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AO4840

40V Dual N-Channel MOSFET

General Description

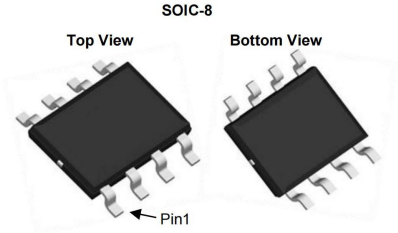
The AO4840 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. This dual device is suitable for use as a load switch or in PWM applications.

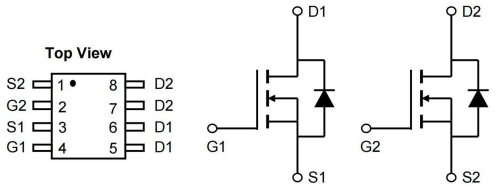
Product Summary

V_{DS}	40V
I_D (at V_{GS}=10V)	6A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 30mΩ
$R_{DS(ON)}$ (at V_{GS}=4.5V)	< 38mΩ

100% UIS Tested
100% R_g Tested

SOIC-8





Orderable Part Number	Package Type	Form	Minimum Order Quantity
	SO-8	Tape & Reel	3000

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A=25°C	I_D	6	A
	T_A=70°C		5	
Pulsed Drain Current [C]		I_{DM}	30	
Avalanche Current [C]		I_{AS}, I_{AR}	14	A
Avalanche energy L=0.1mH [C]		E_{AS}, E_{AR}	10	mJ
Power Dissipation [B]	T_A=25°C	P_D	2	W
	T_A=70°C		1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	48	62.5	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		74	90	°C/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	32	40	°C/W

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Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V			1	μA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250μA	1.7	2.5	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=6A		24	30	mΩ
		T_J=125°C		36	45	
		V_{GS}=4.5V, I_D=5A		30	38	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=6A		27		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.76	1	V
I_S	Maximum Body-Diode Continuous Current				2	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=20V, f=1MHz	410	516	650	pF
C_{oss}	Output Capacitance		55	82	110	pF
C_{rss}	Reverse Transfer Capacitance		25	43	60	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	2.3	4.6	6.9	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=20V, I_D=6A		8.9	10.8	nC
Q_g(4.5V)	Total Gate Charge			4.3	5.6	nC
Q_{gs}	Gate Source Charge			2.4		nC
Q_{gd}	Gate Drain Charge			1.4		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=20V, R_L=3.3Ω, R_{GEN}=3Ω		6.4		ns
t_r	Turn-On Rise Time			3.6		ns
$t_{D(off)}$	Turn-Off DelayTime			16.2		ns
t_f	Turn-Off Fall Time			6.6		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=6A, dI/dt=100A/μs		18	24	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=6A, dI/dt=100A/μs		10		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initialT_J=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

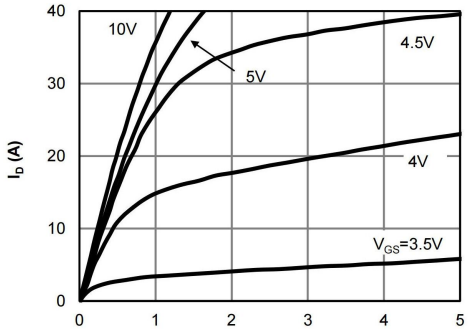


Fig 1: On-Region Characteristics (Note E)

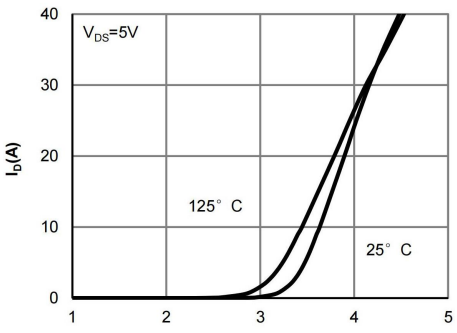


Figure 2: Transfer Characteristics (Note E)

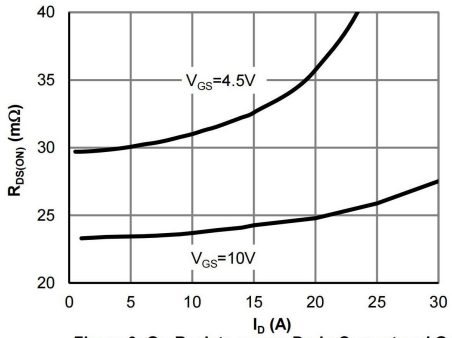


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

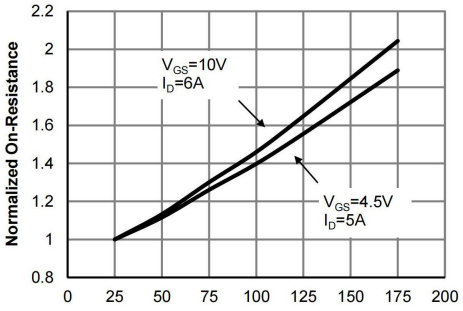


Figure 4: On-Resistance vs. Junction Temperature (Note E)

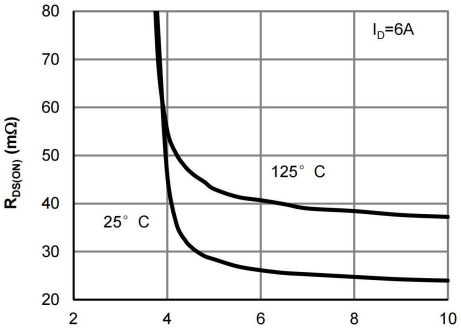


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

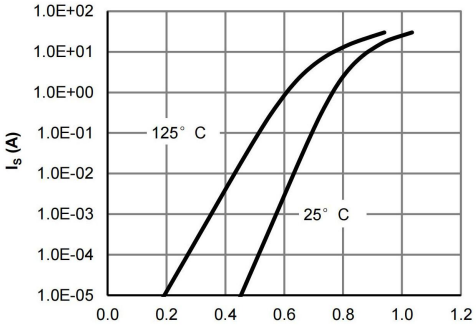


Figure 6: Body-Diode Characteristics (Note E)

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

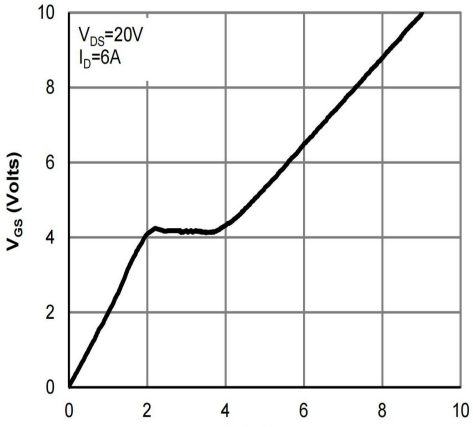


Figure 7: Gate-Charge Characteristics

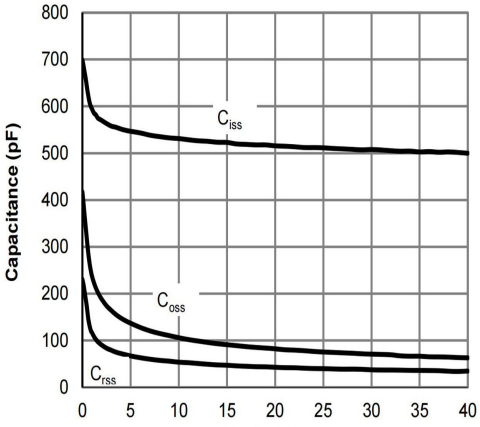


Figure 8: Capacitance Characteristics

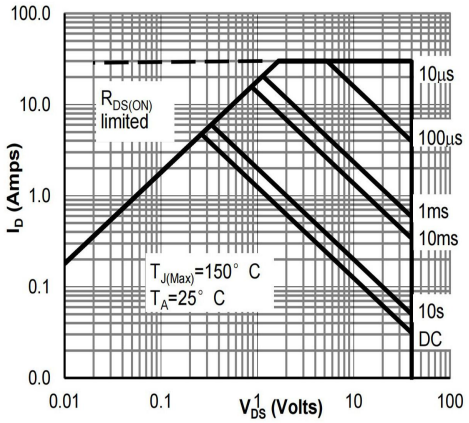


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

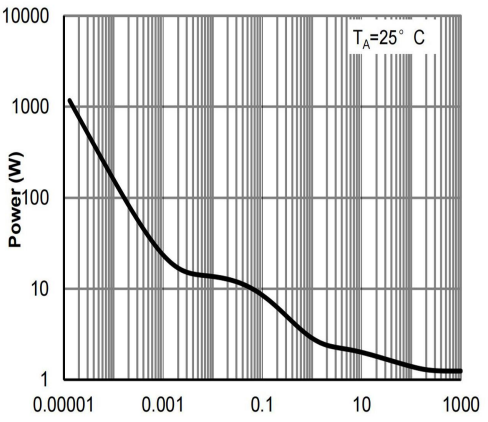


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

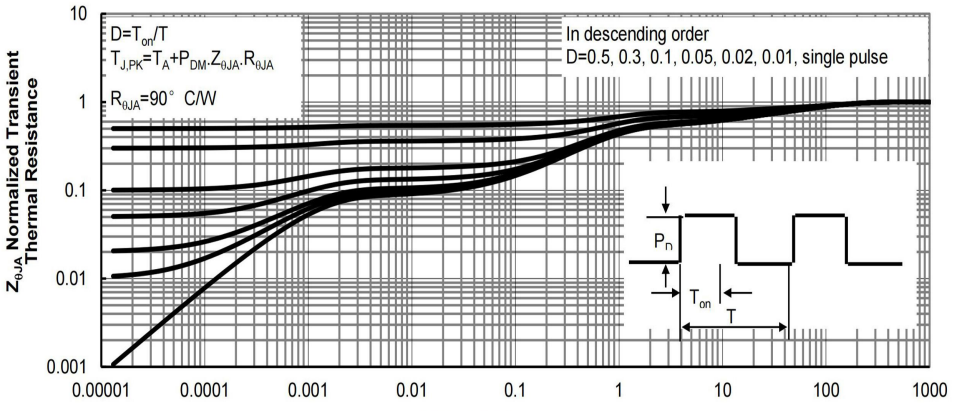
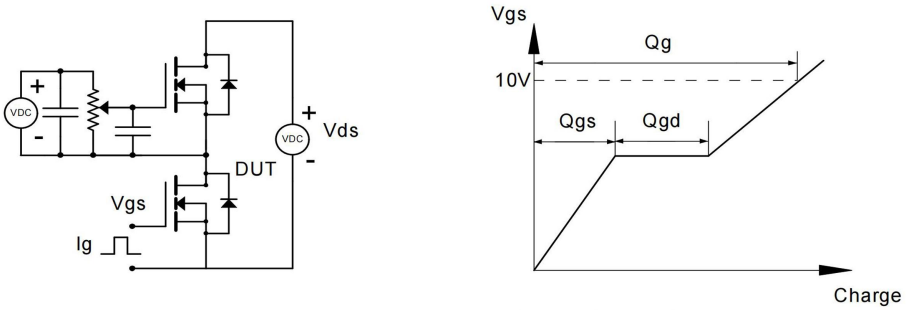


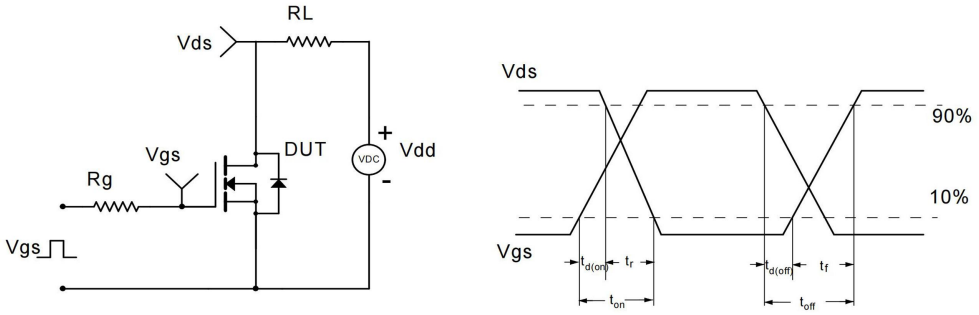
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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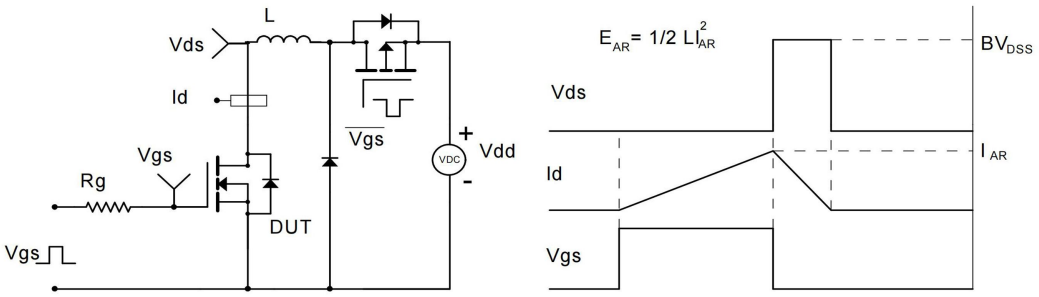
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

