# OM SENI

## AOD4132
## N-Channel Enhancement Mode Field Effect Transistor

### General Description

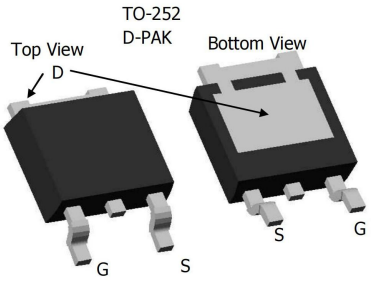
The AOD4132 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and low gate resistance. This device is ideally suited for use as a low side switch in CPU core power conversion.

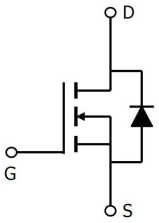
-RoHS Compliant
-Halogen Free*

### Features

$V_{DS}$ (V) = 30V
$I_D$ = 85A ($V_{GS}$ = 10V)
$R_{DS(ON)}$ < 4mΩ ($V_{GS}$ = 10V)
$R_{DS(ON)}$ < 6mΩ ($V_{GS}$ = 4.5V)

***100% UIS Tested!***
***100% Rg Tested!***




| Orderable Part Number | Package Type | Form | Minimum Order Quantity |
|---|---|---|---|
| | TO-252 | Tape & Reel | 2500 |

**Absolute Maximum Ratings $T_A$=25℃ unless otherwise noted**

| Parameter | | Symbol | Maximum | Units |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 30 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current [B,G] | $T_C$=25℃ [G] | $I_D$ | 85 | A |
| | $T_C$=100℃ [B] | | 63 | |
| Pulsed Drain Current | | $I_{DM}$ | 200 | |
| Avalanche Current [C] | | $I_{AR}$ | 30 | A |
| Repetitive avalanche energy L=0.1mH [C] | | $E_{AR}$ | 112 | mJ |
| Power Dissipation [B] | $T_C$=25℃ | $P_D$ | 100 | W |
| | $T_C$=100℃ | | 50 | |
| Power Dissipation [A] | $T_A$=25℃ | $P_{DSM}$ | 2.5 | W |
| | $T_A$=70℃ | | 1.6 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 175 | ℃ |

**Thermal Characteristics**

| Parameter | | Symbol | Typ | Max | Units |
|---|---|---|---|---|---|
| Maximum Junction-to-Ambient [A] | t ≤ 10s | $R_{\theta JA}$ | 14.2 | 20 | ℃/W |
| Maximum Junction-to-Ambient [A] | Steady-State | | 39 | 50 | ℃/W |
| Maximum Junction-to-Case [C] | Steady-State | $R_{\theta JC}$ | 0.8 | 1.5 | ℃/W |

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**Electrical Characteristics ($T_J$=25℃ unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=250μA, $V_{GS}$=0V | 30 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=24V, $V_{GS}$=0V | | | 1 | μA |
| | | $T_J$=55℃ | | | 5 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$= ±20V | | | 100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$ $I_D$=250μA | 1 | 1.8 | 3 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}$=10V, $V_{DS}$=5V | 85 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=10V, $I_D$=20A | | 2.8 | 4 | mΩ |
| | | $T_J$=125℃ | | 4.4 | 5.5 | |
| | | $V_{GS}$=4.5V, $I_D$=20A | | 4.4 | 6 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=5V, $I_D$=20A | | 106 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=1A,$V_{GS}$=0V | | 0.72 | 1 | V |
| $I_S$ | Maximum Body-Diode Continuous Current | | | | 85 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=15V, f=1MHz | | 3700 | 4400 | pF |
| $C_{oss}$ | Output Capacitance | | | 700 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 390 | | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | | 0.54 | 0.7 | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$(10V) | Total Gate Charge | $V_{GS}$=4.5V, $V_{DS}$=15V, $I_D$=20A | | 63 | 76 | nC |
| $Q_g$(4.5V) | Total Gate Charge | | | 33 | 40 | nC |
| $Q_{gs}$ | Gate Source Charge | | | 8.6 | | nC |
| $Q_{gd}$ | Gate Drain Charge | | | 17.6 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=10V, $V_{DS}$=15V, $R_L$=0.75Ω, $R_{GEN}$=3Ω | | 12 | | ns |
| $t_r$ | Turn-On Rise Time | | | 15.5 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 40 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 14 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=20A, dI/dt=100A/μs | | 34 | 41 | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=20A, dI/dt=100A/μs | | 30 | | nC |

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25℃. The Power dissipation $P_{DSM}$ is based on steady-state $R_{\theta JA}$ and the maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design, and the maximum temperature fo 175℃ may be u sed if the PCB or heatsink allows it.

B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=175℃, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175℃.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These tests are performed with the device mounted on 1 in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25℃. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by the package current capability.

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## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

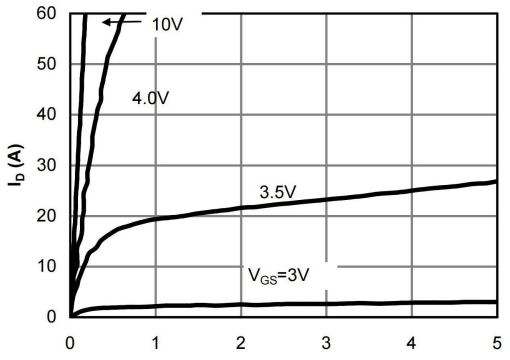



Fig 1: On-Region Characteristics

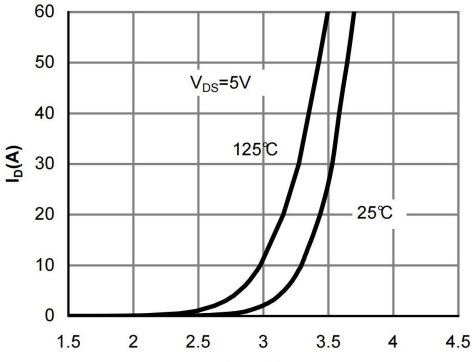



Figure 2: Transfer Characteristics

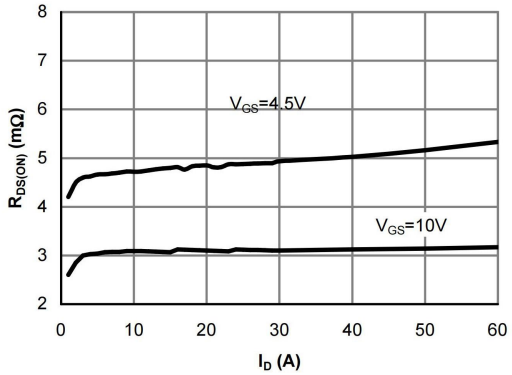



Figure 3: On-Resistance vs. Drain Current and Gate Voltage

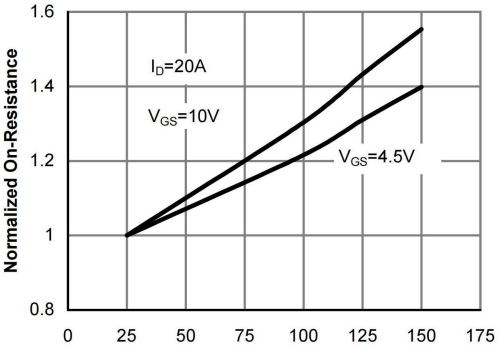



Figure 4: On-Resistance vs. Junction Temperature

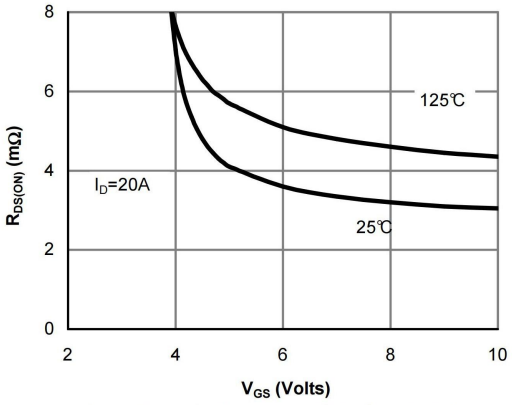



Figure 5: On-Resistance vs. Gate-Source Voltage

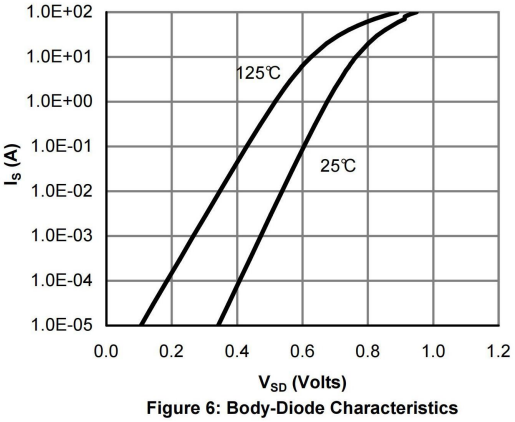



Figure 6: Body-Diode Characteristics

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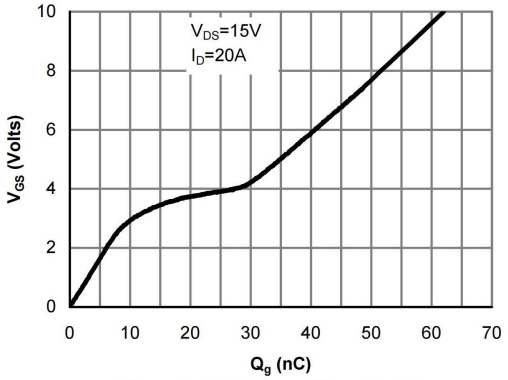



Figure 7: Gate-Charge Characteristics

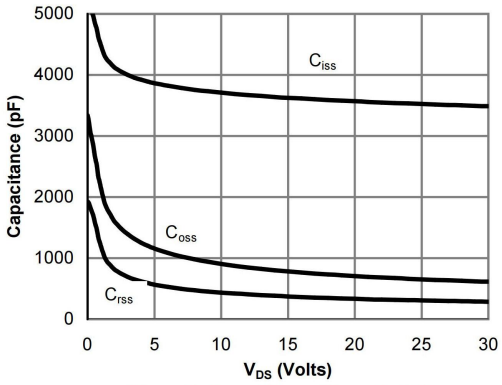



Figure 8: Capacitance Characteristics

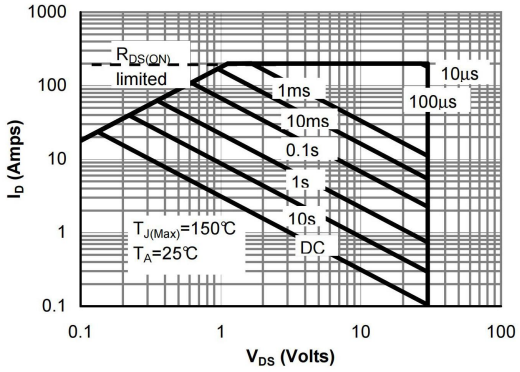



Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

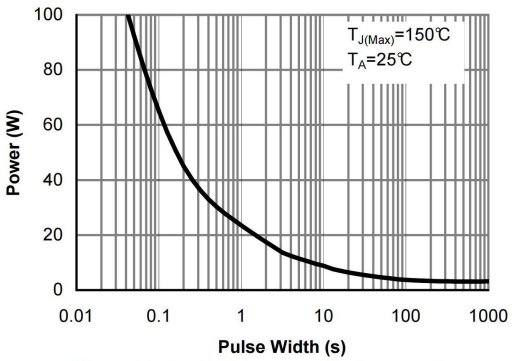



Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

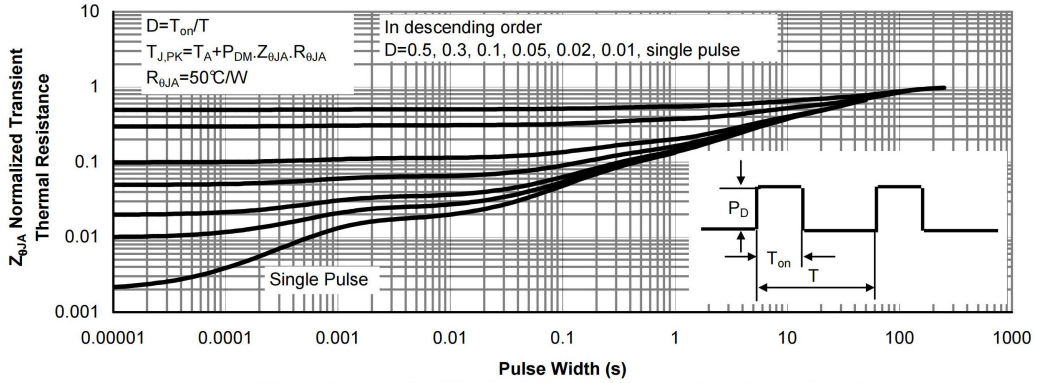



Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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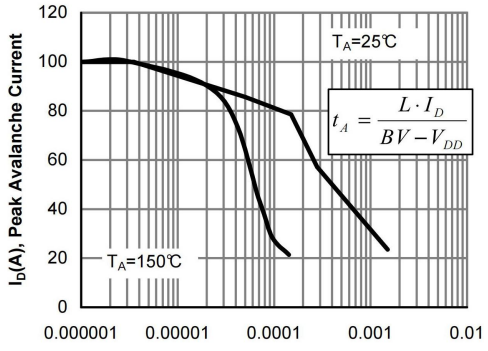



Figure 12: Single Pulse Avalanche capability

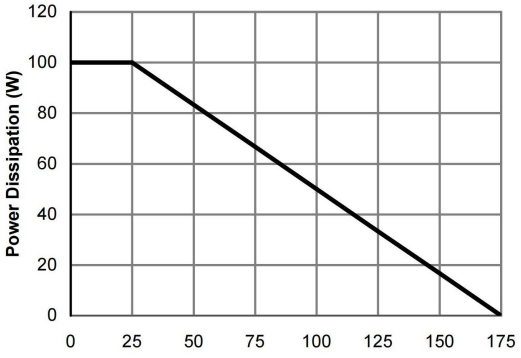



Figure 13: Power De-rating (Note B)

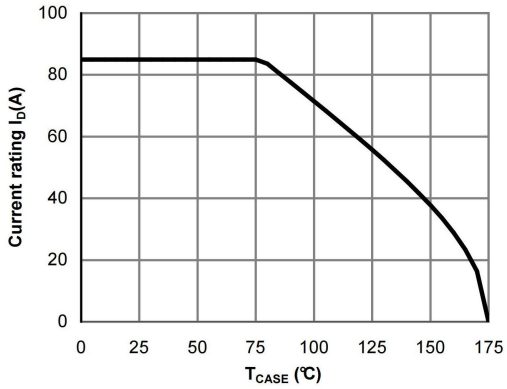
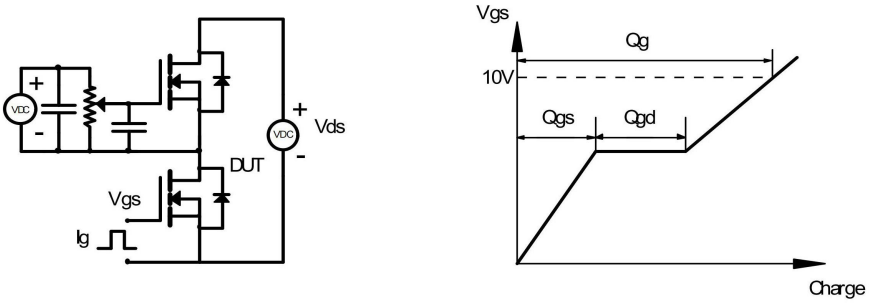


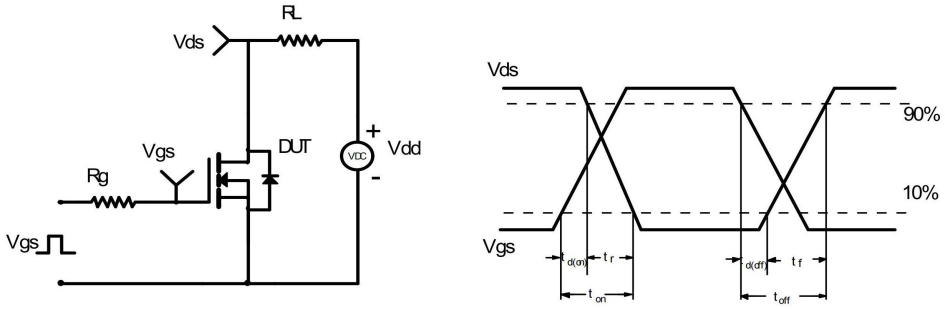

Figure 14: Current De-rating (Note B)

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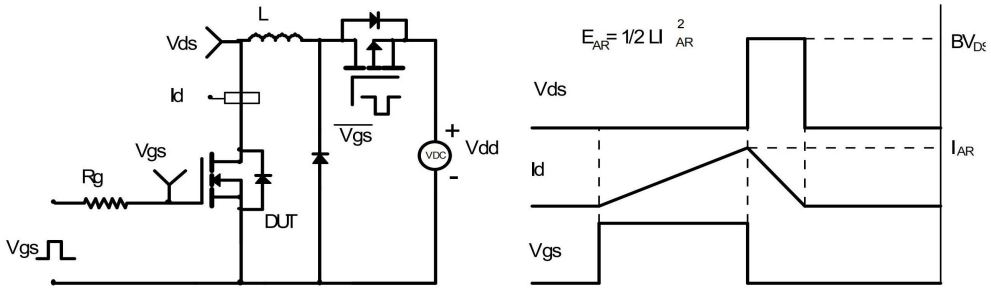
Gate Charge Test Circuit & Waveform




Resistive Switching Test Circuit & Waveforms




Unclamped Inductive Switching (UIS) Test Circuit & Waveforms




Diode Recovery Test Circuit & Waveforms

