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AOD4185
P-Channel Enhancement Mode Field Effect Transistor

General Description

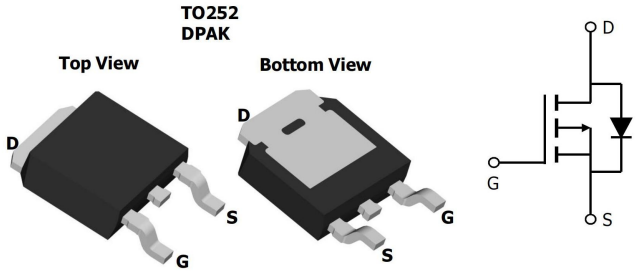
The AOD4185 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. With the excellent thermal resistance of the DPAK/IPAK package, this device is well suited for high current applications.

-RoHS Compliant
-Halogen Free*

Features

V_{DS} (V) = -40V
I_D = -40A (V_{GS} = -10V)
$R_{DS(ON)}$ < 15mΩ (V_{GS} = -10V)
$R_{DS(ON)}$ < 20mΩ (V_{GS} = -4.5V)

100% UIS Tested!
100% Rg Tested!



Orderable Part Number	Package Type	Form	Minimum Order Quantity
	TO-252	Tape & Reel	2500

Absolute Maximum Ratings T_C=25℃ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [B,H]	T_C=25℃	I_D	-40	A
	T_C=100℃		-31	
Pulsed Drain Current [C]		I_{DM}	-115	
Avalanche Current [C]		I_{AR}	-42	
Repetitive avalanche energy L=0.1mH [C]		E_{AR}	88	mJ
Power Dissipation [B]	T_C=25℃	P_D	62.5	W
	T_C=100℃		31	
Power Dissipation [A]	T_A=25℃	P_{DSM}	2.5	
	T_A=70℃		1.6	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	℃

Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A,G]	t ≤ 10s	$R_{\theta JA}$	15	20	℃/W
Maximum Junction-to-Ambient [A,G]	Steady-State		41	50	℃/W
Maximum Junction-to-Case [D,F]	Steady-State	$R_{\theta JC}$	2	2.4	℃/W

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Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250μA, V_{GS}=0V	-40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-40V, V_{GS}=0V			-1	μA
		T_J=55℃			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250μA	-1.7	-1.9	-3	V
$I_{D(ON)}$	On state drain current	V_{GS}=-10V, V_{DS}=-5V	-115			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-20A		12.5	15	mΩ
		T_J=125℃		19	23	
		V_{GS}=-4.5V, I_D=-15A		16	20	
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-20A		50		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.72	-1	V
I_S	Maximum Body-Diode Continuous Current				-20	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-20V, f=1MHz		2550		pF
C_{oss}	Output Capacitance			280		pF
C_{rss}	Reverse Transfer Capacitance			190		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	2.5	4	6	Ω
SWITCHING PARAMETERS						
Q_g (-10V)	Total Gate Charge	V_{GS}=-10V, V_{DS}=-20V, I_D=-20A		42	55	nC
Q_g (-4.5V)	Total Gate Charge			18.6		
Q_{gs}	Gate Source Charge			7		nC
Q_{gd}	Gate Drain Charge			8.6		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-20V, R_L=1Ω, R_{GEN}=3Ω		9.4		ns
t_r	Turn-On Rise Time			20		ns
$t_{D(off)}$	Turn-Off DelayTime			55		ns
t_f	Turn-Off Fall Time			30		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-20A, dI/dt=100A/μs		38	49	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-20A, dI/dt=100A/μs		47		nC

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

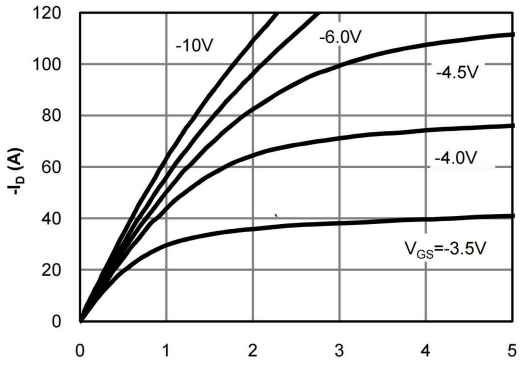


Figure 1: On-Region Characteristics

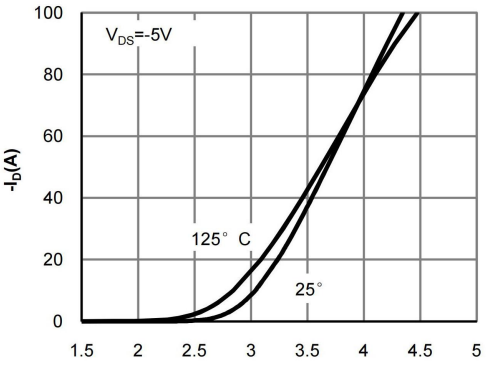


Figure 2: Transfer Characteristics

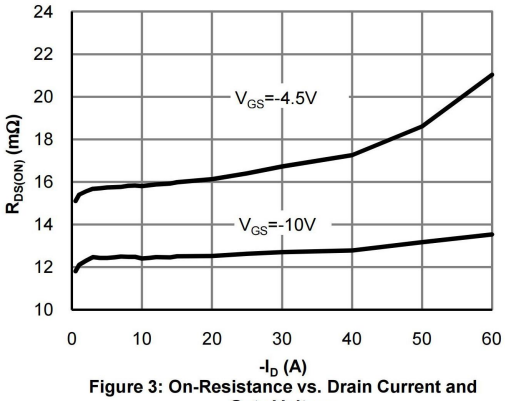


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

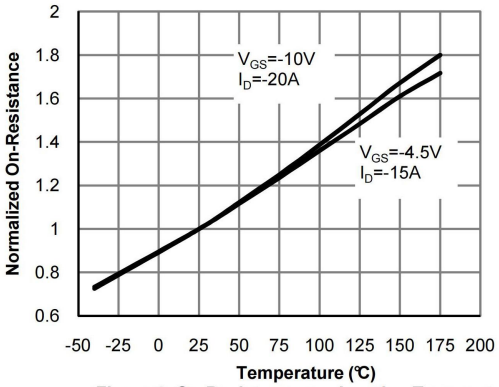


Figure 4: On-Resistance vs. Junction Temperature

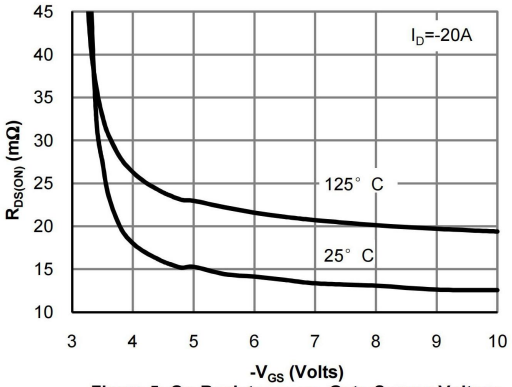


Figure 5: On-Resistance vs. Gate-Source Voltage

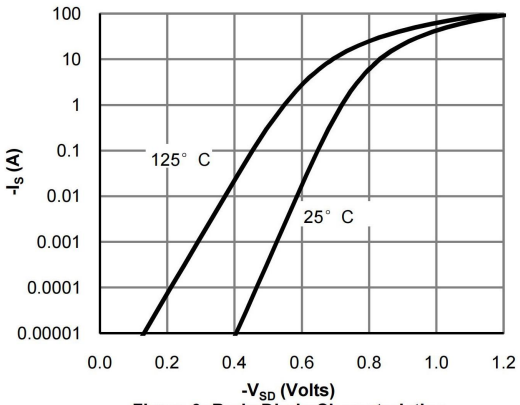


Figure 6: Body-Diode Characteristics

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

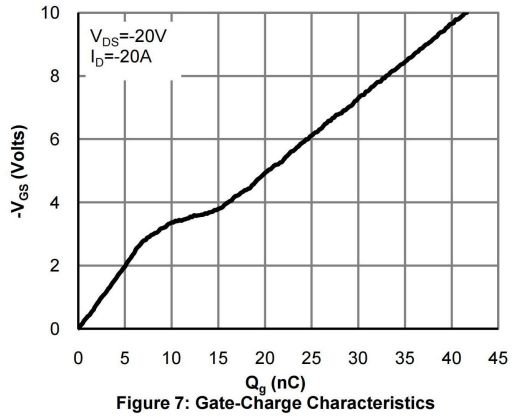


Figure 7: Gate-Charge Characteristics

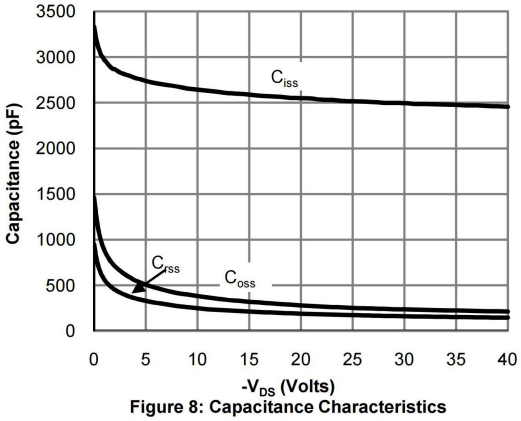


Figure 8: Capacitance Characteristics

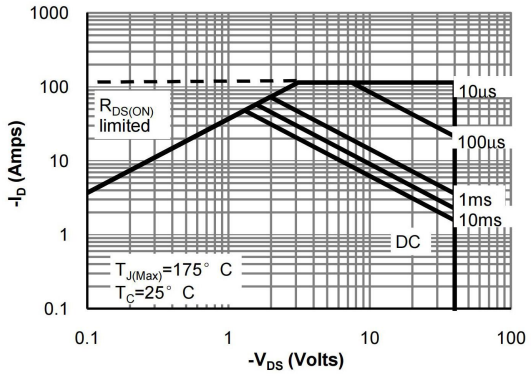


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

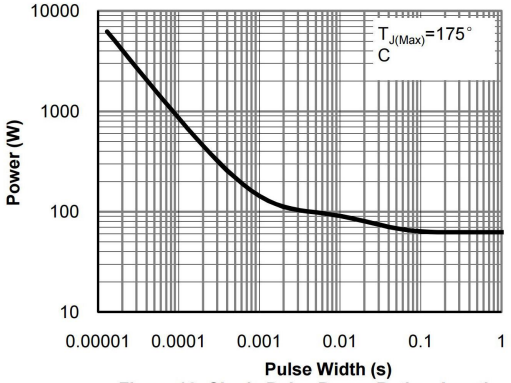


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

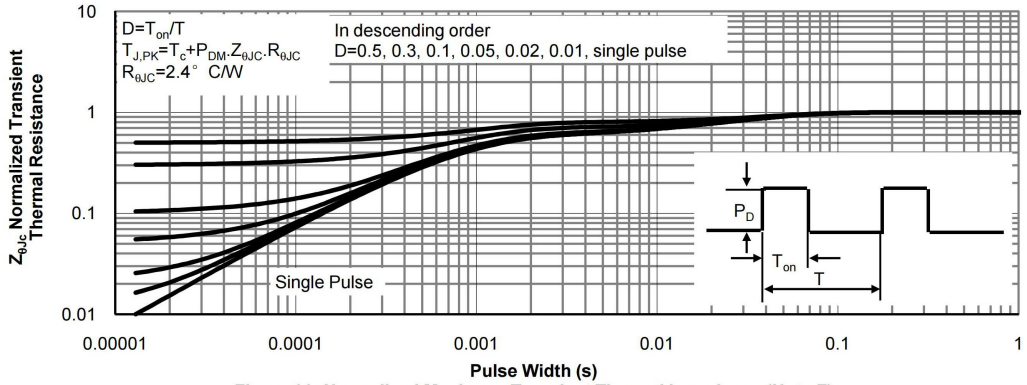


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

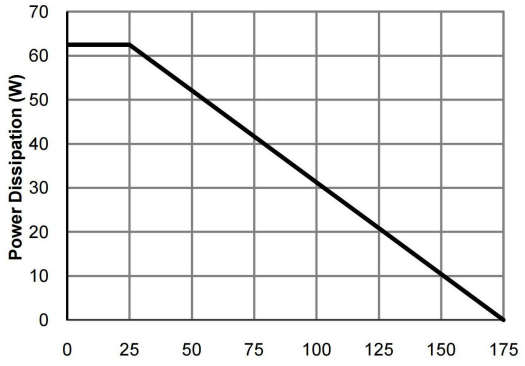


Figure 12: Power De-rating (Note B)

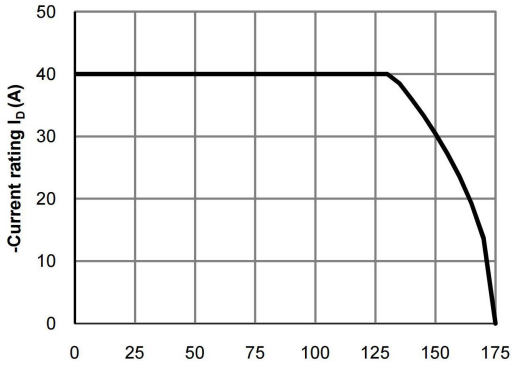


Figure 13: Current De-rating (Note B)

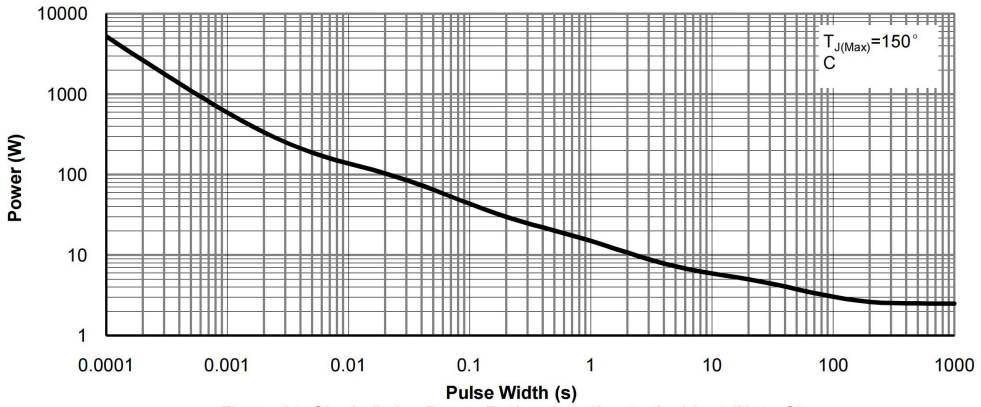


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

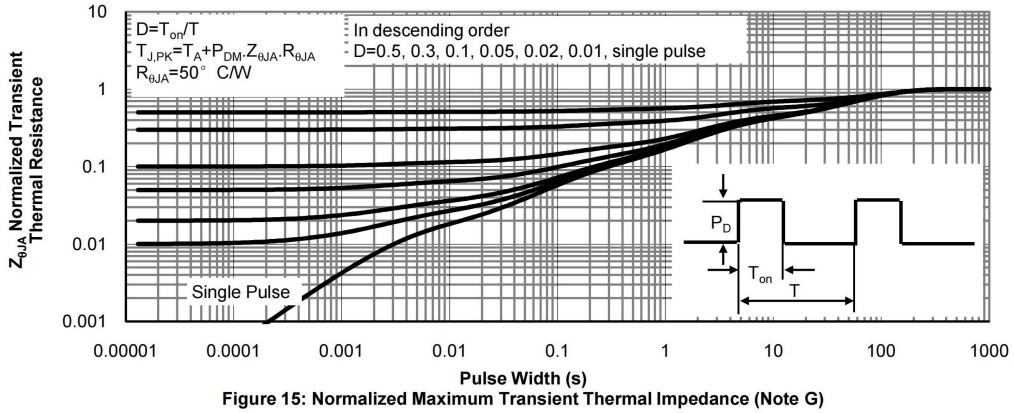
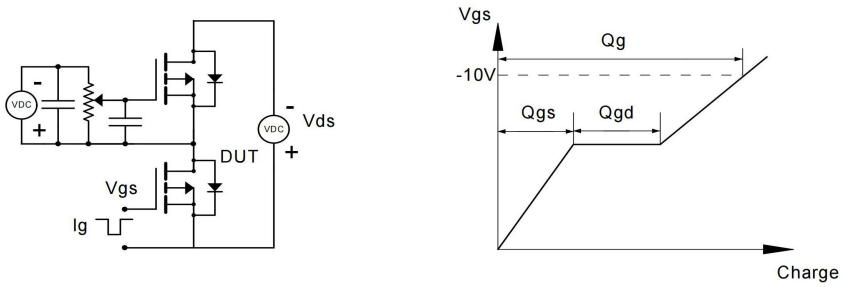


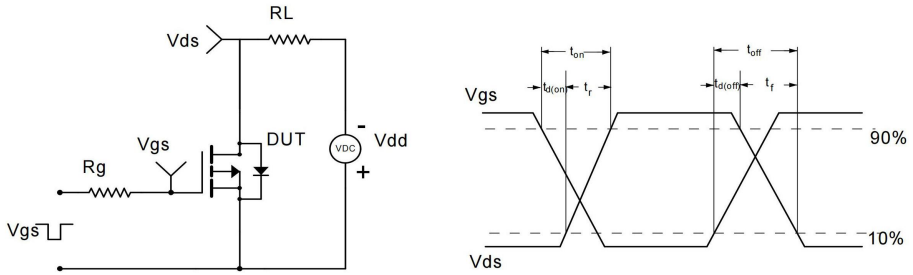
Figure 15: Normalized Maximum Transient Thermal Impedance (Note G)

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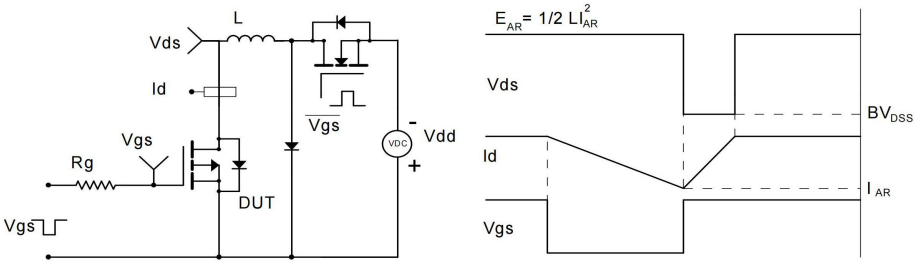
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

