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AOD450

200V N-Channel MOSFET

General Description

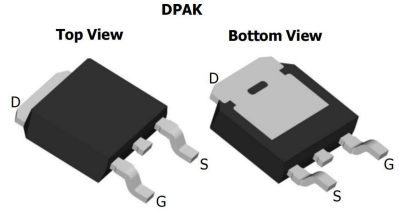
The AOD450 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in inverter, load switching and general purpose applications.

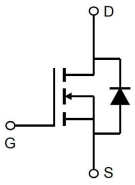
Product Summary

V_{DS}	200V
I_D (at V_{GS}=10V)	3.8A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 0.70Ω

100% UIS Tested
100% R_g Tested

TO252
DPAK





Orderable Part Number	Package Type	Form	Minimum Order Quantity
	TO-252	Tape & Reel	2500

Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	T_C=25℃	I_D	3.8	A
	T_C=100℃		2.7	
Pulsed Drain Current [C]		I_{DM}	10	
Avalanche Current [C]		I_{AS}	3	A
Avalanche energy L=1.35mH [C]		E_{AS}	6	mJ
Power Dissipation [B]	T_C=25℃	P_D	25	W
	T_C=100℃		12.5	
Power Dissipation [A]	T_A=25℃	P_{DSM}	2.1	W
	T_A=70℃		1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	℃

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	17.1	30	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		50	60	℃/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	4	6	℃/W

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Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=10mA, V_{GS}=0V	200			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=160V, V_{GS}=0V			1	μA
		T_J=55℃			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±30V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	3	5	6	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=3.8A		0.55	0.7	Ω
		T_J=125℃		1.1	1.32	
g_{FS}	Forward Transconductance	V_{DS}=15V, I_D=3.8A		8.7		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.8	1	V
I_S	Maximum Body-Diode Continuous Current [G]				6	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz	170	215	260	pF
C_{oss}	Output Capacitance		20	32	50	pF
C_{rss}	Reverse Transfer Capacitance		3	7.2	15	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		5.5		Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=25V, I_D=3.8A		3.82		nC
Q_g(4.5V)	Total Gate Charge			0.92		nC
Q_{gs}	Gate Source Charge			1.42		nC
Q_{gd}	Gate Drain Charge			1.47		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=25V, R_L=6.5Ω, R_{GEN}=3Ω		6.3		ns
t_r	Turn-On Rise Time			3.3		ns
$t_{D(off)}$	Turn-Off DelayTime			10.5		ns
t_f	Turn-Off Fall Time			2.8		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=3.8A, dI/dt=100A/μs		59		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=3.8A, dI/dt=100A/μs		142		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175° C. Ratings are based on low frequency and duty cycles to keep initial T_J =25° C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

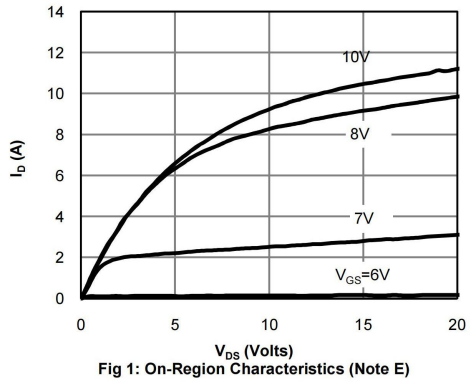


Fig 1: On-Region Characteristics (Note E)

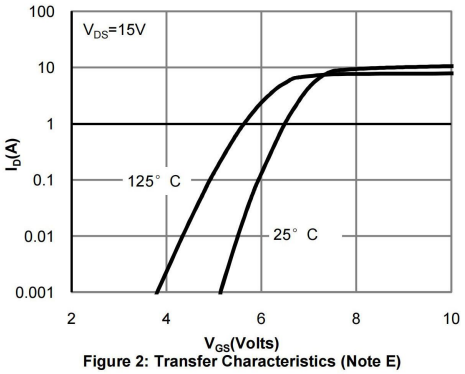


Figure 2: Transfer Characteristics (Note E)

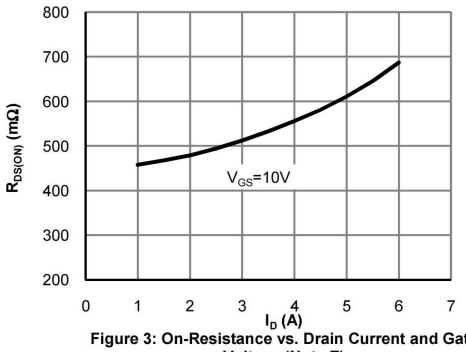


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

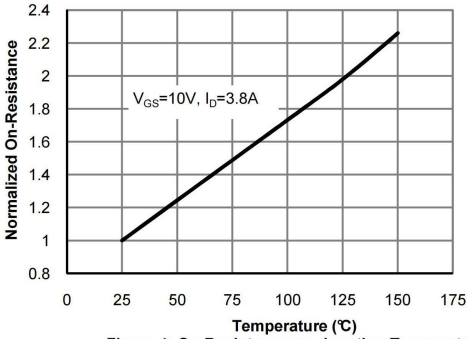


Figure 4: On-Resistance vs. Junction Temperature (Note E)

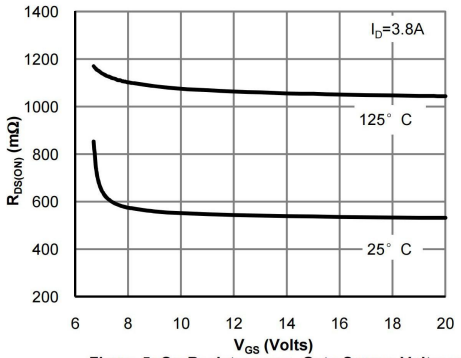


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

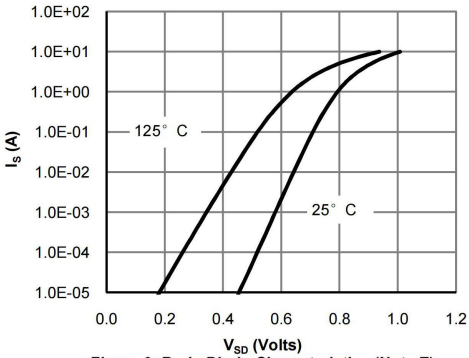


Figure 6: Body-Diode Characteristics (Note E)

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

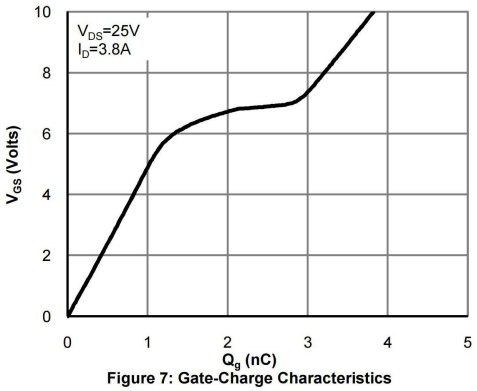


Figure 7: Gate-Charge Characteristics

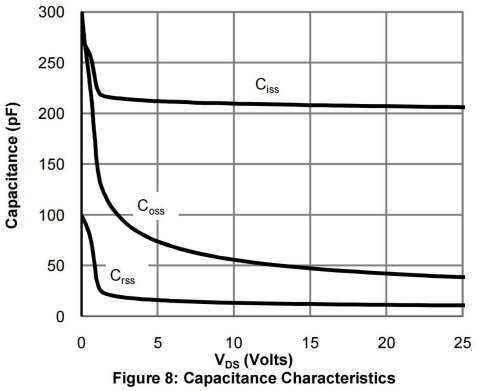


Figure 8: Capacitance Characteristics

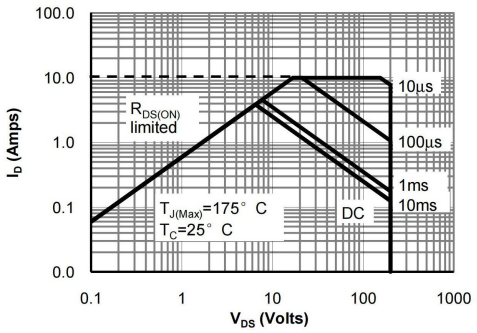


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

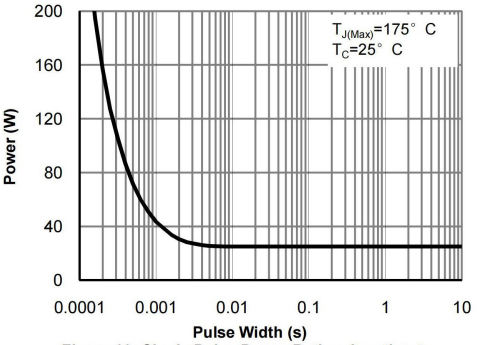


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

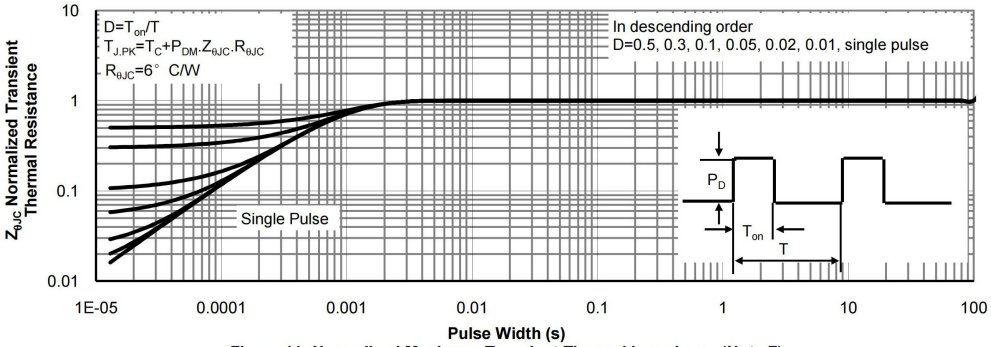


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

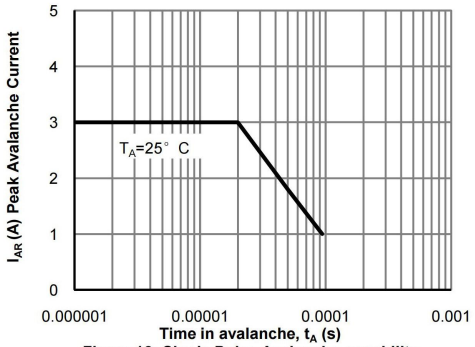


Figure 12: Single Pulse Avalanche capability (Note C)

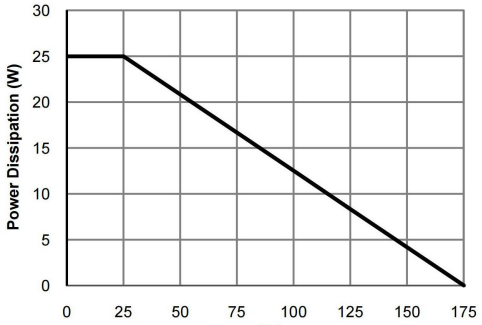


Figure 13: Power De-rating (Note F)

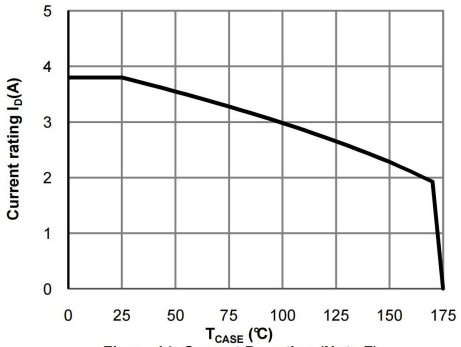


Figure 14: Current De-rating (Note F)

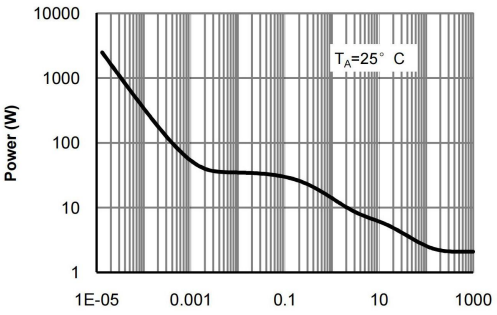


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

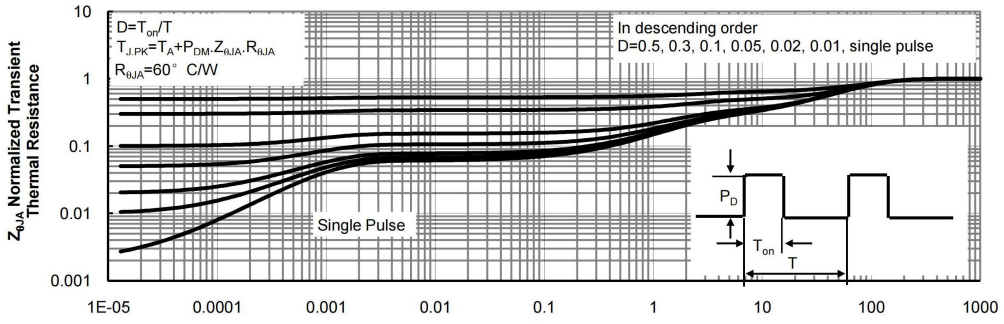
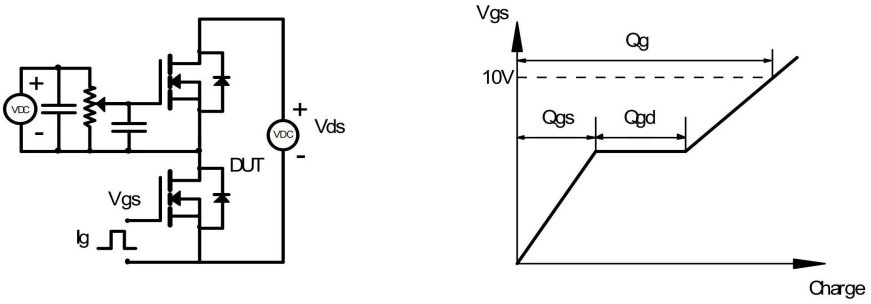


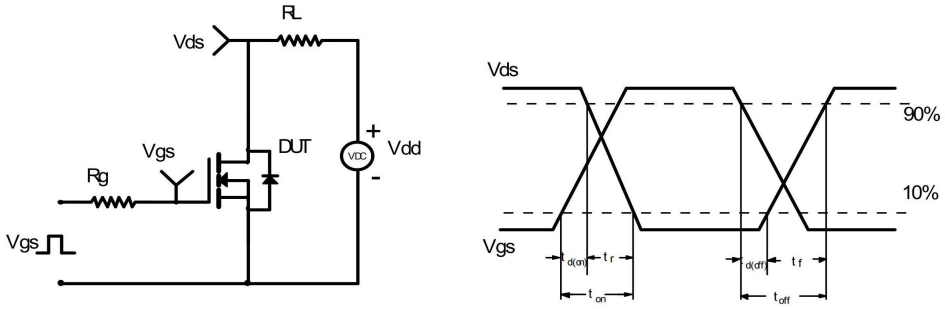
Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

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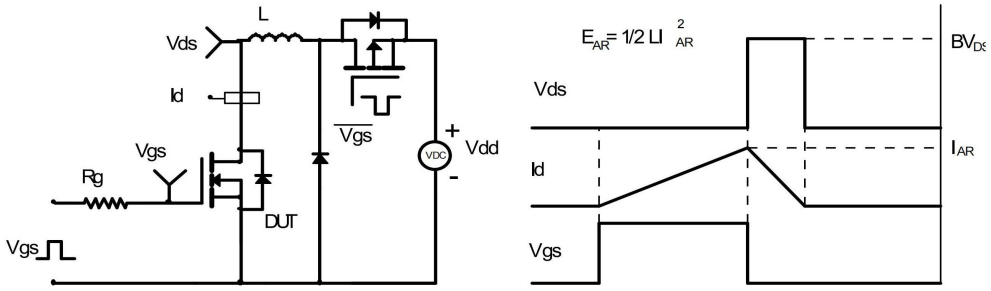
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

