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AOD464
N-Channel Enhancement Mode Field Effect Transistor

General Description

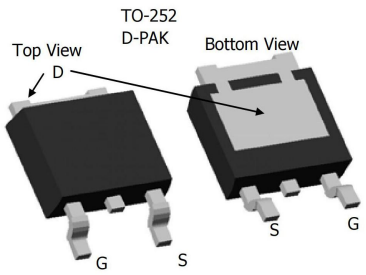
The AOD464 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in high voltage synchronous rectification , load switching and general purpose applications.

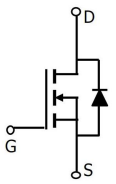
-RoHS Compliant
-Halogen Free*

Features

V_{DS} (V) = 105V
I_D = 40 A (V_{GS} =10V)
$R_{DS(ON)}$ < 28 mΩ (V_{GS} =10V) @ 20A
$R_{DS(ON)}$ < 31 mΩ (V_{GS} = 6V)

100% UIS Tested!
100% Rg Tested!





Orderable Part Number	Package Type	Form	Minimum Order Quantity
	TO-252	Tape & Reel	2500

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	105	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current	T_C=25°C	I_D	40	A
	T_C=100°C		28	
Pulsed Drain Current [C]		I_{DM}	80	
Avalanche Current [C]		I_{AR}	20	A
Repetitive avalanche energy L=0.1mH [C]		E_{AR}	20	mJ
Power Dissipation [B]	T_C=25°C	P_D	100	W
	T_C=100°C		50	
Power Dissipation [A]	T_A=25°C	P_{DSM}	2.3	W
	T_A=70°C		1.5	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	15	18	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		45	55	°C/W
Maximum Junction-to-Case [B]	Steady-State	$R_{\theta JC}$	1	1.5	°C/W

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Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=10mA, V_{GS}=0V	105			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=84V, V_{GS}=0V			1	μA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±25V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2.5	3.2	4	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	80			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		21.5	28	mΩ
		T_J=125°C		32	40	
		V_{GS}=6V, I_D=20A		24	31	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		50		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.73	1	V
I_S	Maximum Body-Diode Continuous Current				55	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz		2038	2445	pF
C_{oss}	Output Capacitance			204		pF
C_{rss}	Reverse Transfer Capacitance			85		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		1.3	1.56	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=50V, I_D=20A		38.5	46	nC
Q_{gs}	Gate Source Charge			8		nC
Q_{gd}	Gate Drain Charge			10		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=50V, R_L=2.7Ω, R_{GEN}=3Ω		12.7		ns
t_r	Turn-On Rise Time			8.2		ns
$t_{D(off)}$	Turn-Off DelayTime			31.5		ns
t_f	Turn-Off Fall Time			11.2		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=100A/μs		59.6	74	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=100A/μs		161		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

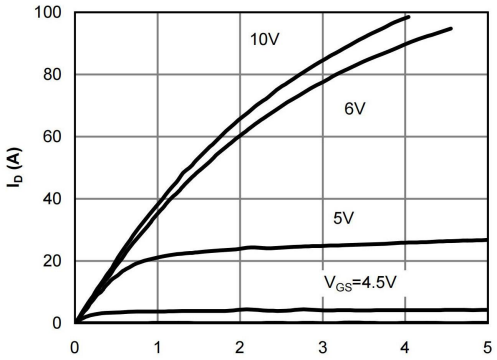


Fig 1: On-Region Characteristics

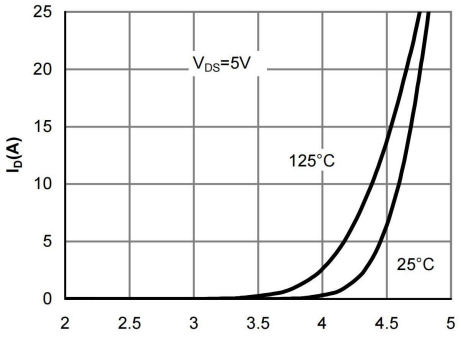


Figure 2: Transfer Characteristics

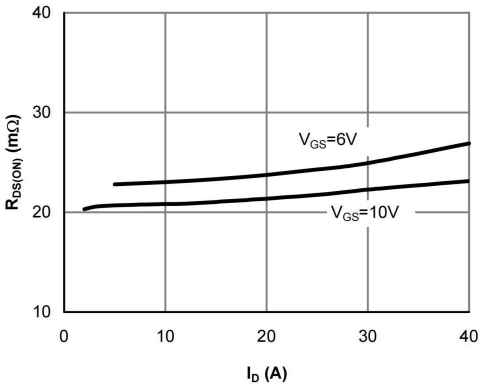


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

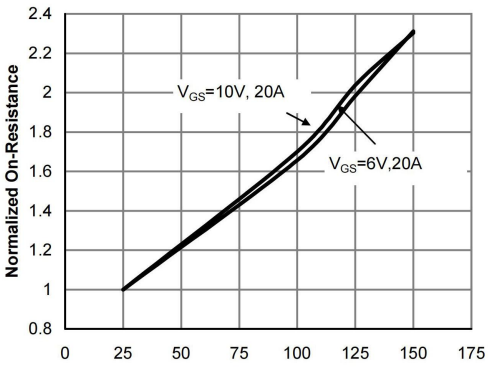


Figure 4: On-Resistance vs. Junction Temperature

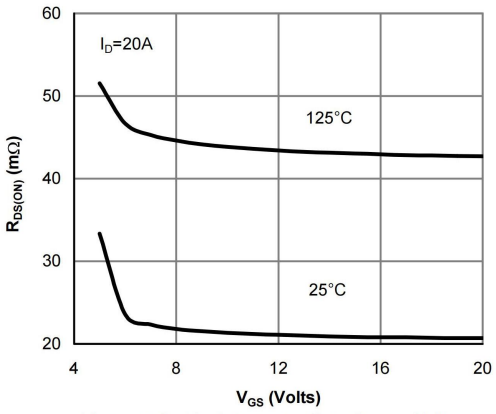


Figure 5: On-Resistance vs. Gate-Source Voltage

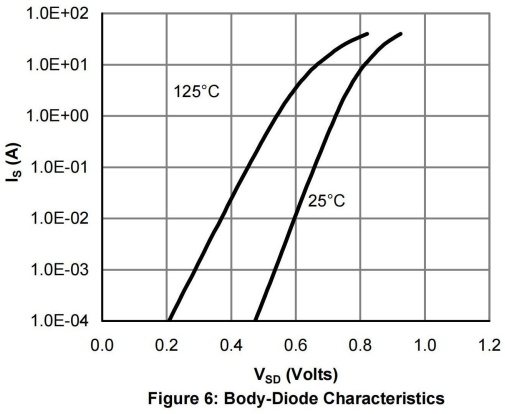


Figure 6: Body-Diode Characteristics

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

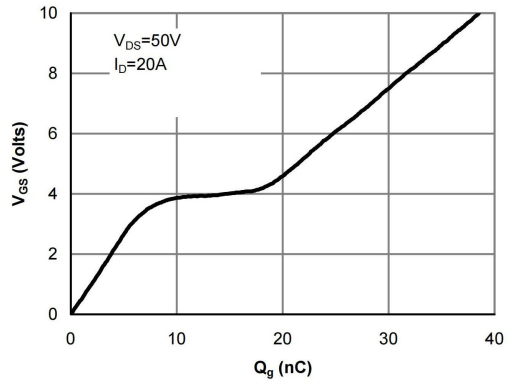


Figure 7: Gate-Charge Characteristics

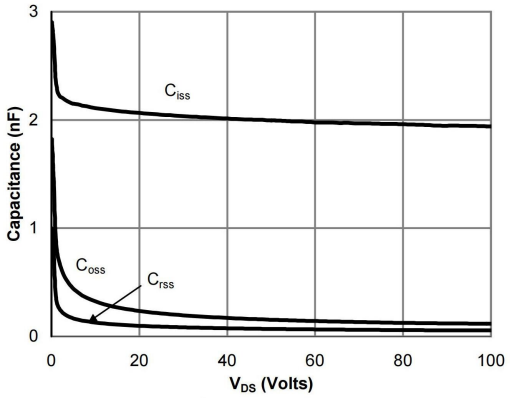


Figure 8: Capacitance Characteristics

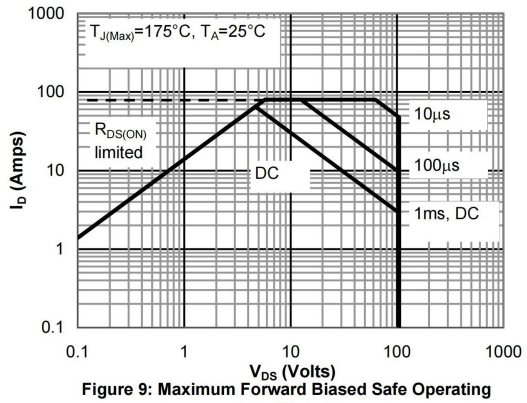


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

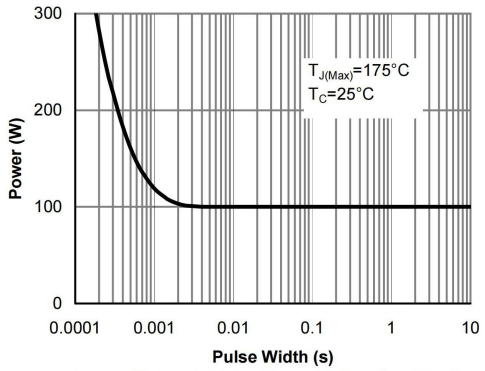


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

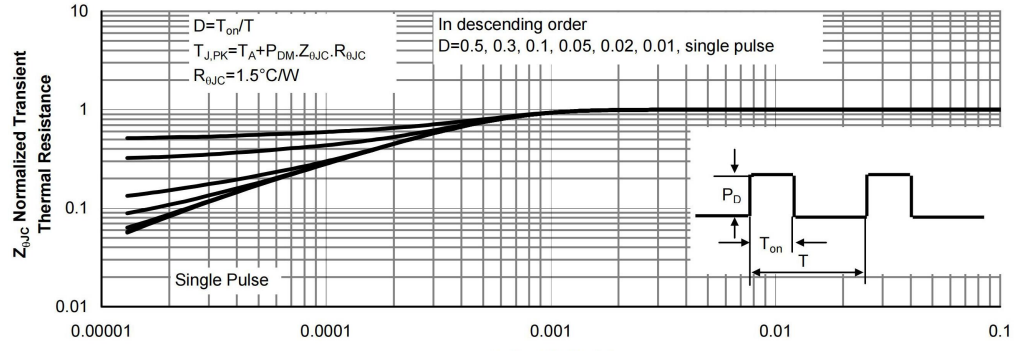


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

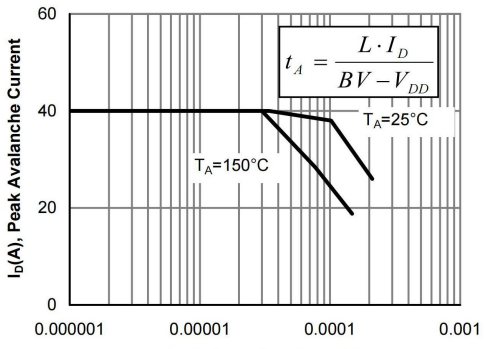


Figure 12: Single Pulse Avalanche capability

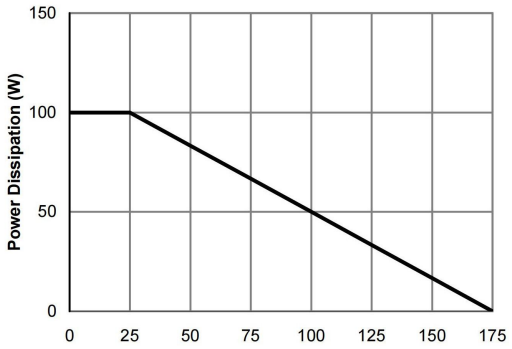


Figure 13: Power De-rating (Note B)

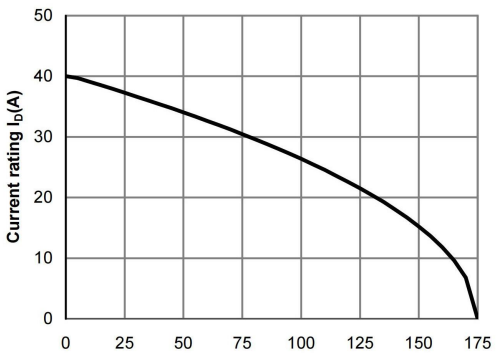


Figure 14: Current De-rating (Note B)

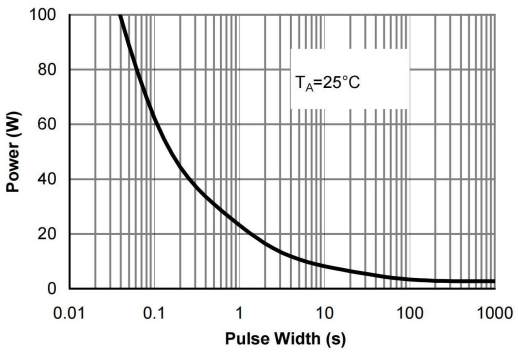


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

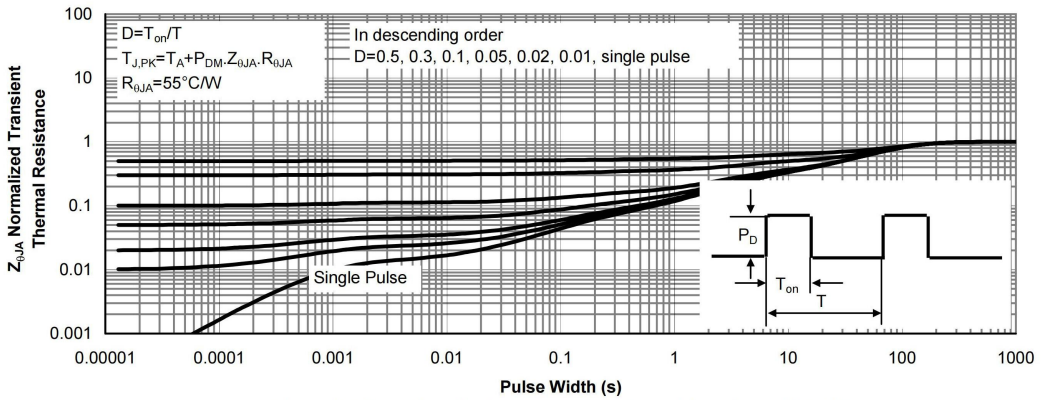
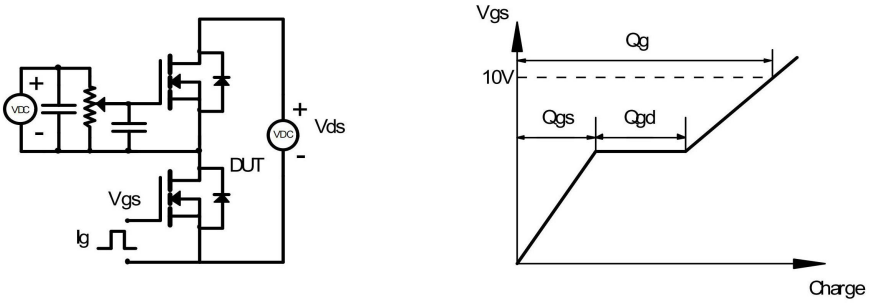


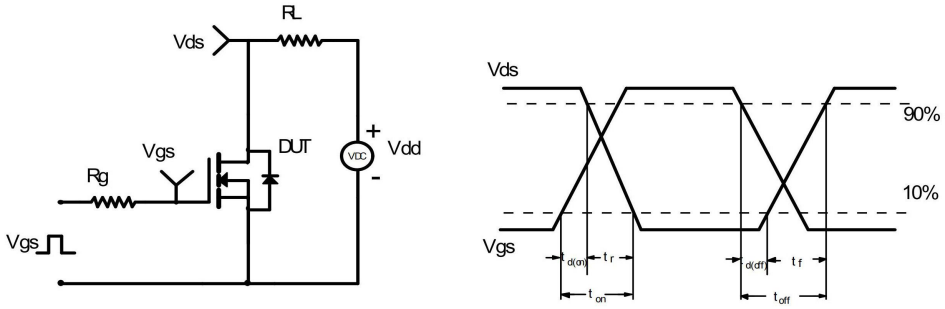
Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

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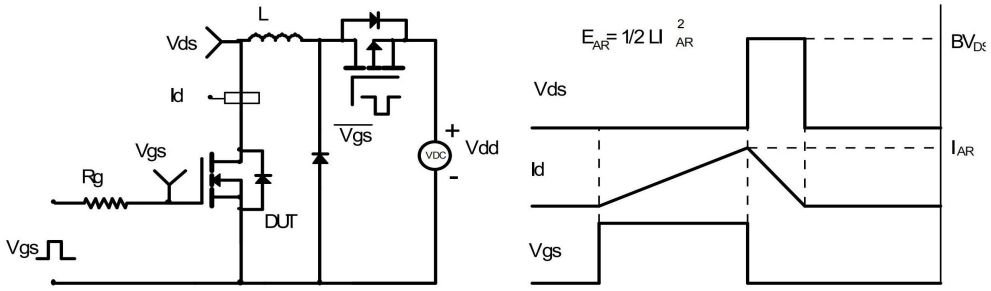
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

