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SPICE Device Model Si2349DS-T1-GE3
P-Channel 20-V (D-S) MOSFET

CHARACTERISTICS

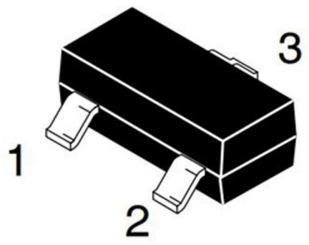
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

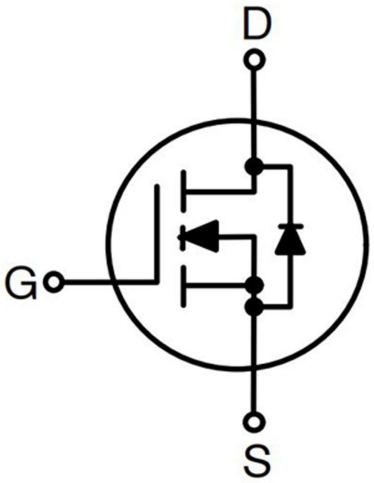
A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



SOT−23

1 – Gate
2 – Source
3 – Drain



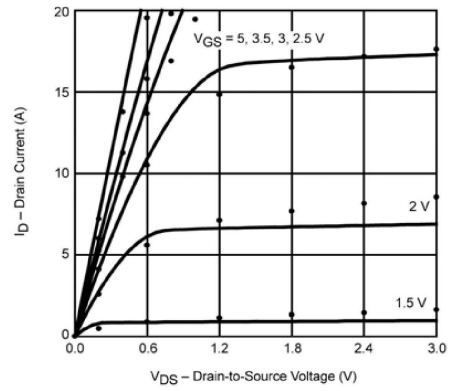
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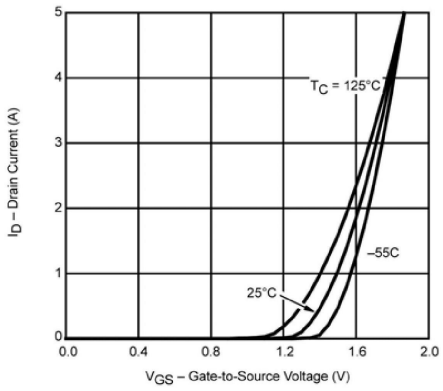
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	**Symbol**	**Test Condition**	**Simulated Data**	**Measured Data**	**Unit**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 μA	0.98		V
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ −5 V, V_{GS} = −4.5 V	94		A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = −4.5 V, I_D = −5.1 A	0.028	0.038	Ω
		V_{GS} = −2.5 V, I_D = −4.1 A	0.048	0.059	
Forward Transconductance[a]	g_{fs}	V_{DS} = −10 V, I_D = −5.1 A	24	13	S
Diode Forward Voltage[a]	V_{SD}	I_S = −2.1 A	−0.81	−0.80	V
Dynamic[b]					
Input Capacitance	C_{iss}	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	840	665	pF
Output Capacitance	C_{oss}		181	177	
Reverse Transfer Capacitance	C_{rss}		114	128	
Total Gate Charge	Q_g	V_{DS} = −10 V, V_{GS} = −5 V, I_D = −5.1A	8	8.6	nC
		V_{DS} = −10 V, V_{GS} = −4.5 V, I_D = −5.1 A	7.3	8	
Gate-Source Charge	Q_{gs}		1.4	1.4	
Gate-Drain Charge	Q_{gd}		3.1	3.1	

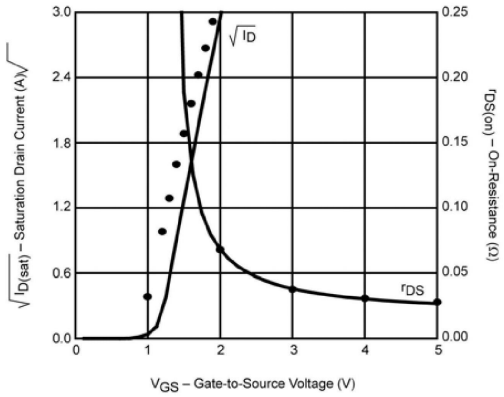
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

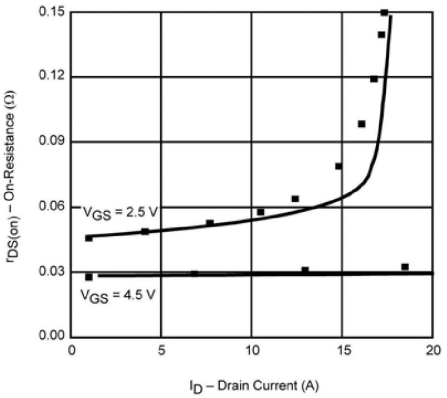
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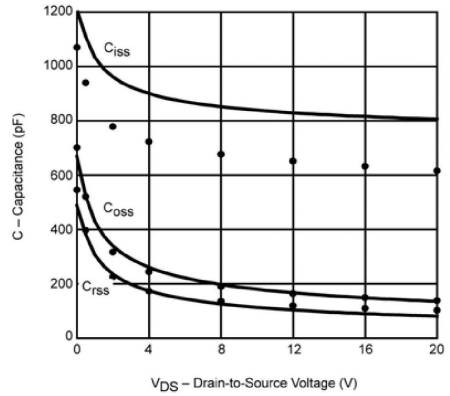
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

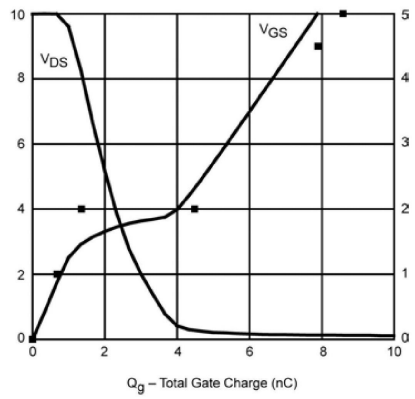












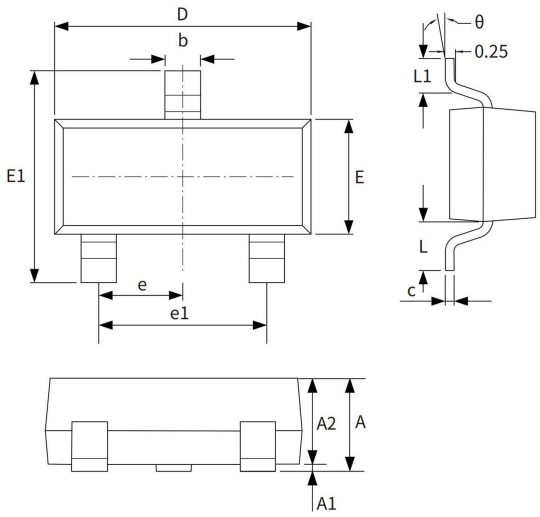
Note: Dots and squares represent measured data.

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Ordering Information

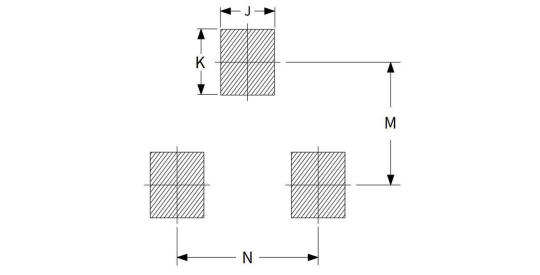
PACKAGE	PACKAGE CODE	UNIT WEIGHT(g)	REEL(pcs)	BOX(pcs)	CARTON(pcs)	DELIVERY MODE
SOT-23	R1	0.008	3000	30000	240000	7''

Package Outline Dimensions (SOT-23)



Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.90	1.15	0.035	0.045
A1	-	0.10	-	0.004
A2	0.90	1.05	0.035	0.041
b	0.30	0.50	0.012	0.020
c	0.10	0.20	0.004	0.008
D	2.80	3.00	0.110	0.118
E	1.20	1.40	0.047	0.055
E1	2.25	2.55	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.80	2.00	0.071	0.079
L	0.550REF		0.022REF	
L1	0.30	0.50	0.012	0.020
θ	-	8°	-	8°

Suggested Pad Layout



Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
J	0.75	0.85	0.030	0.033
K	0.85	0.95	0.033	0.037
M	1.95	2.05	0.077	0.081
N	1.85	1.95	0.073	0.077